# CLOVER DISPLAY LTD.

# LCD MODULE SPECIFICATION

## Model : ZCG12864R - _ _ - _ _ - _ _ -

| | |
|---|---|
| Revision | 00 |
| Engineering | PANWU |
| Date | 23 JAN 13 |
| Our Reference | |


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## *MODE OF DISPLAY*

| Display mode | Display condition | Viewing direction |
|---|---|---|
| STN : ☐ Yellow green | ☐ Reflective type | ☐ 6 O' clock |
| ☐ Grey | ☐ Transflective type | ☐ 12 O' clock |
| ☐ Blue (negative) | ☐ Transmissive type | ☐ 3 O' clock |
| ☐ FSTN positive | ☐ Others | ☐ 9 O' clock |
| ☐ FSTN negative | | |

## *LCD MODULE NUMBER NOTATION:*

ZCG12864R - N N - S F - N 6 – T
(1) (2) (3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
T – TN
V – TN (Negative)
S – STN Yellow green
G – STN Grey
B – STN Blue (Negative)
F – FSTN
N – FSTN (Negative)
*(5)---Rear polarizer type
R – Reflective
F – Transflective
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)

## GENERAL DESCRIPTION

Display mode : 128 x 64 dots, graphic COG LCD module

Interface : Serial

Driving method : 1/64 duty, 1/9 bias

Controller IC : Sitronix SPLC502B or equivalence
For the detailed information, please refer to the IC specifications.

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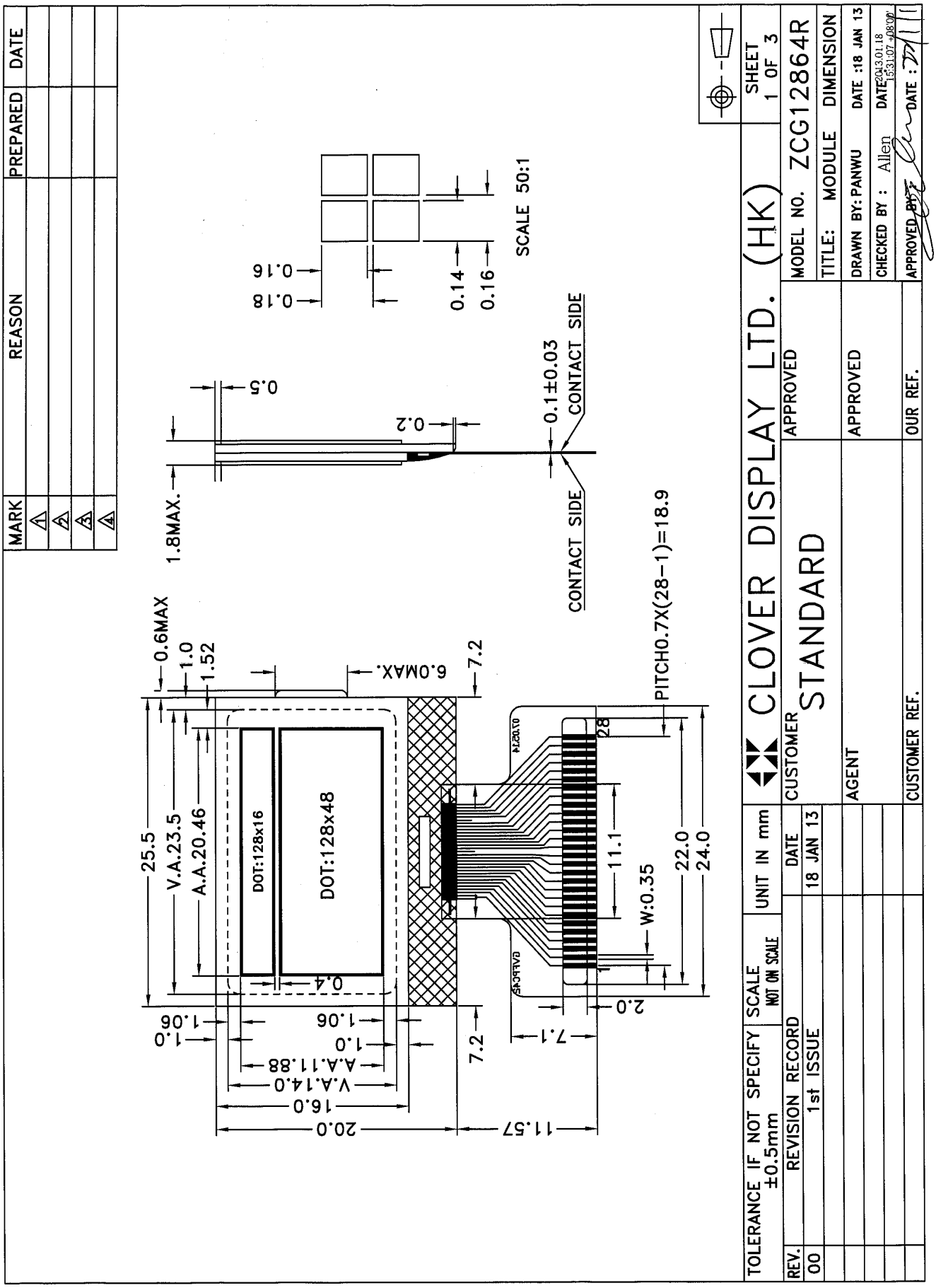
## MECHANICAL DIMENSIONS

| Item | Dimension | Unit | Item | Dimension | Unit |
|---|---|---|---|---|---|
| Outline Dimension | 25.5(L)x 20.0(W)x 1.8MAX. (H) | mm | Dot Pitch | 0.16(L)x0.18(W) | mm |
| Viewing Area | 23.5(L)x 14.0(W) | mm | Dot Size | 0.14(L)x0.16(W) | mm |

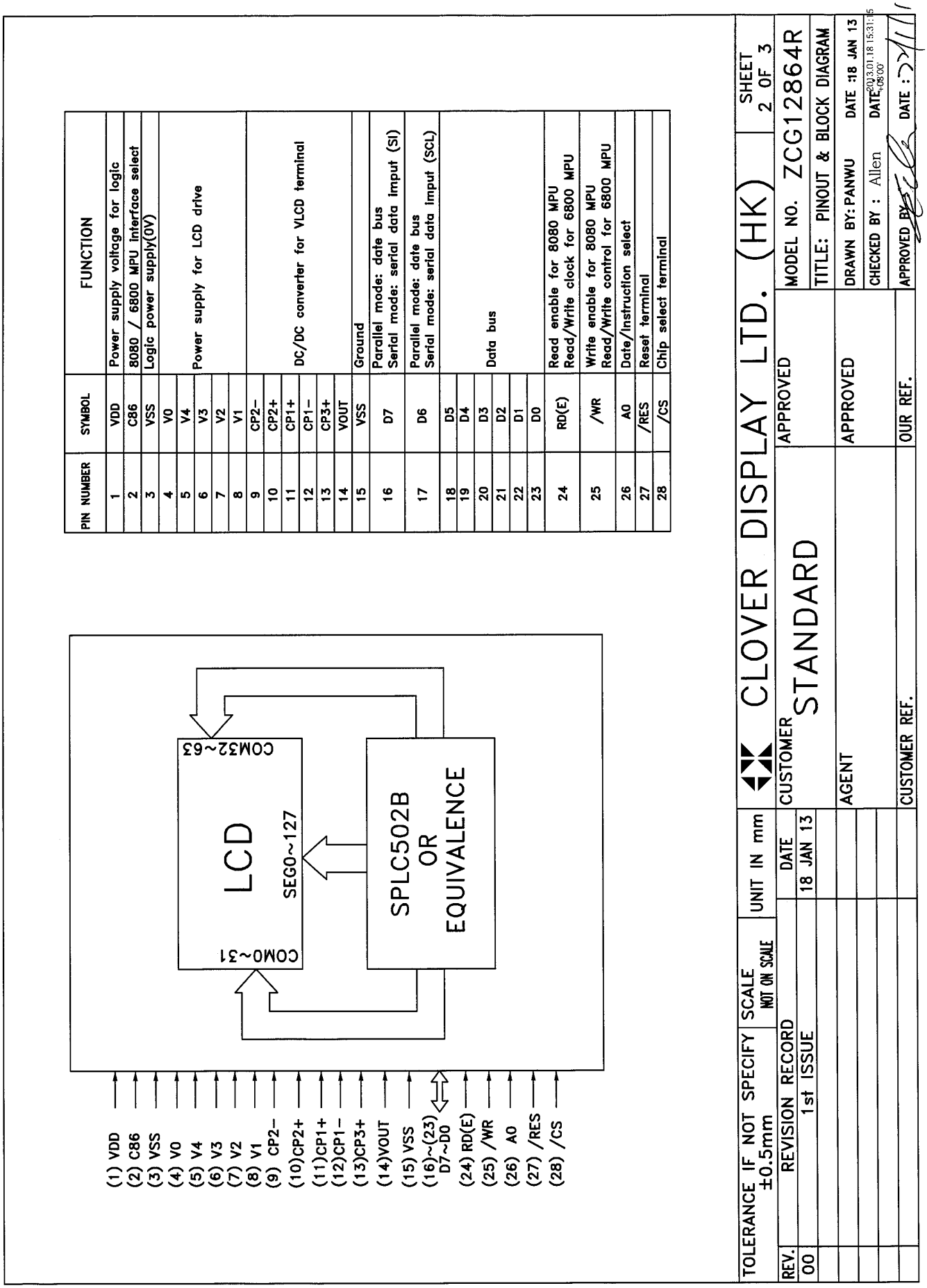
### CONNECTOR PIN ASSIGNMENT

| Pin No. | Symbol | Function | Pin No. | Symbol | Function |
|---|---|---|---|---|---|
| 1 | VDD | Power supply voltage for logic | 15 | VSS | Ground |
| 2 | C86 | 8080 / 6800 MPU interface select | 16 | D7 | Parallel mode: date bus<br>Serial mode: serial data imput (SI) |
| 3 | VSS | Logic power supply(0V) | 17 | D6 | Parallel mode: date bus<br>Serial mode: serial data imput (SCL) |
| 4 | V0 | Power supply for LCD drive | 18 | D5 | Data bus |
| 5 | V4 | | 19 | D4 | |
| 6 | V3 | | 20 | D3 | |
| 7 | V2 | | 21 | D2 | |
| 8 | V1 | | 22 | D1 | |
| 9 | CP2- | DC/DC converter for VLCD terminal | 23 | D0 | |
| 10 | CP2+ | | 24 | RD(E) | Read enable for 8080 MPU<br>Read/Write clock for 6800 MPU |
| 11 | CP1+ | | 25 | /WR | Write enable for 8080 MPU<br>Read/Write control for 6800 MPU |
| 12 | CP1- | | 26 | A0 | Date/Instruction select |
| 13 | CP3+ | | 27 | /RES | Reset terminal |
| 14 | VOUT | | 28 | /CS | Chip select terminal |

# COUNTER DRAWING OF MODULE DIMENSION



# COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



## LECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

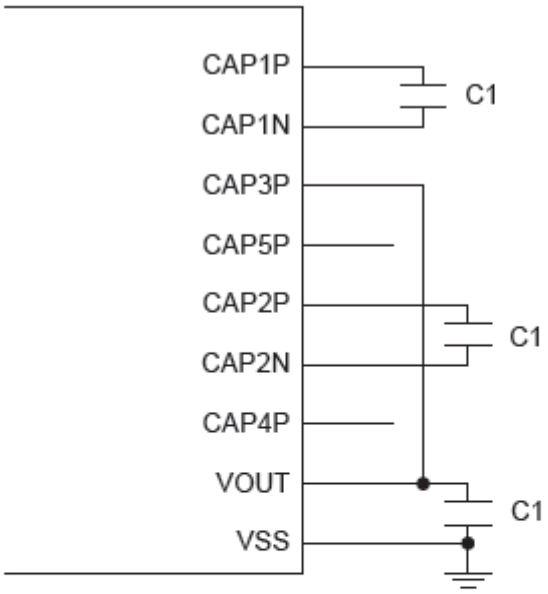
| Item | Symbol | MIN. | TYP. | MAX. | Unit |
|---|---|---|---|---|---|
| Supply Voltage for Logic | VDD | 2.75 | 3.0 | 3.25 | V |
| Supply Current for Logic | IDD | — | 130 | 160 | uA |
| Operating Voltage for LCD(*) | VLCD | 7.6 | 8.0 | 8.4 | V |
| 'High' Level Input Voltage | VIH | 0.8VDD | — | VDD | V |
| 'Low' Level Input Voltage | VIL | VSS | — | 0.2VDD | V |

**Note (*): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.**

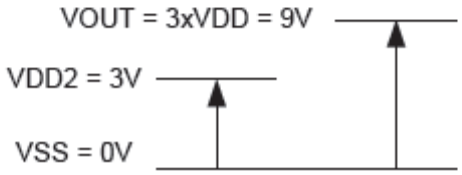
## ABSOLUTE MAXIMUM RATINGS

| Parameter | | Symbol | Conditions | Unit |
|---|---|---|---|---|
| Power supply voltage | | VDD | -0.3~3.6 | v |
| Power supply voltage ( VDD standard ) | | VDD2 | -0.3~3.0 | V |
| Power supply voltage ( VDD standard ) | | V0,Vlcd | -0.3~+12 | V |
| Power supply voltage ( VDD standard ) | | V1,V2,V3,V4 | -0.3 to V0 | V |
| Operating temperature | | TOPR | -20 to 75 | ˚C |
| Storage temperature | Bare chip | TSTR | -55 to +125 | ˚C |

**REFERENCE CIRCUIT EXAMPLE**




3 X (VDD - VSS)

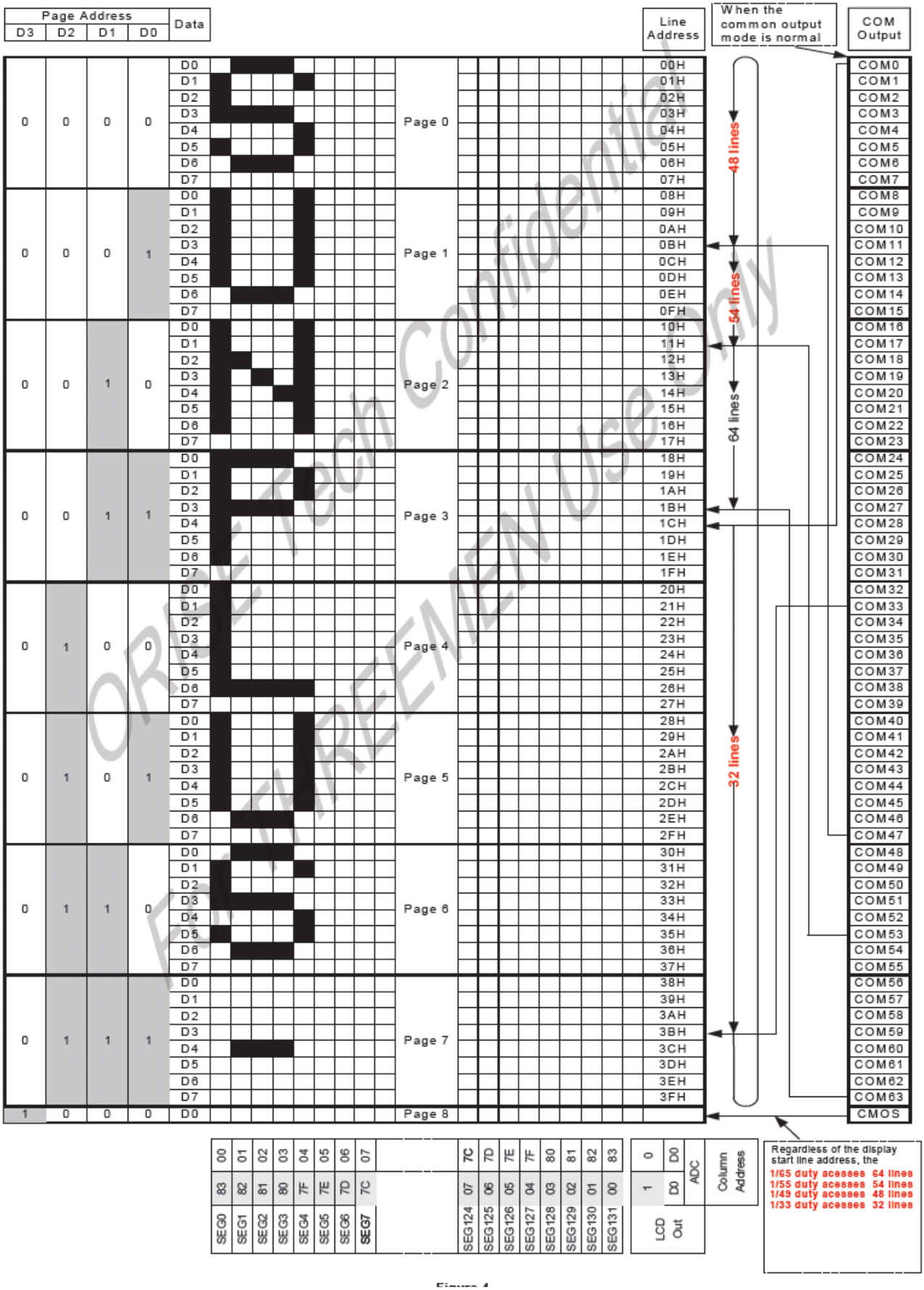


# INSTRUCTIONS

| Command | Command Code | | | | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | A0P | $\overline{RD}$ | $\overline{WR}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| 1). Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0<br>1 | LCD display ON/OFF<br>0: OFF, 1: ON |
| 2). Display start line set | 0 | 1 | 0 | 0 | 1 | Display start address | | | | | | Sets the display RAM display start line address |
| 3). Page address set | 0 | 1 | 0 | 1 | 0 | 1 | 1 | Page address | | | | Sets the display RAM page address |
| 4). Column address set upper bit | 0 | 1 | 0 | 0 | 0 | 0 | 1 | Most significant column address | | | | Sets the most significant 4 bits of the display RAM column address. |
| Column address set lower bit | 0 | 1 | 0 | 0 | 0 | 0 | 0 | Least significant column address | | | | Set the least significant 4 bits of the display RAM column address. |
| 5). Status read | 0 | 0 | 1 | Status | | | | 0 | 0 | 0 | 0 | Reads the status data |
| 6). Display data write | 1 | 1 | 0 | Write data | | | | | | | | Writes to the display RAM |
| 7). Display data read | 1 | 0 | 1 | Read data | | | | | | | | Reads from the display RAM |
| 8). ADC select | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0<br>1 | Sets the display RAM address SEG output correspondence<br>0: normal, 1:reverse |
| 9). Display normal/reverse | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0<br>1 | Sets the LCD display normal/ reverse<br>0: normal, 1:reverse |
| 10). Display all points ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0<br>1 | Display all points<br>0: normal display<br>1: all points ON |
| 11). LCD bias set | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0<br>1 | Sets the LCD driver voltage bias ratio<br>SPLC502B.....0:1/9, 1:1/7 |
| 12). Read/modify/write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Column address increment<br>At write: +1<br>At read: 0 |
| 13). End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Clear read/modify/write |
| 14). Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Internal reset |
| 15). Common output mode select | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0<br>1 | * | * | * | Select COM output scan direction<br>0: normal direction,<br>1: reverse direction |
| 16). Power control set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | Operating mode | | | Select internal power supply operating mode |
| 17). V0 voltage regulator internal resistor ratio set | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | Resistor ratio | | | Select internal resistor ratio (Rb/Ra) mode |
| 18). Electronic volume mode set | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | Set the V0 output voltage electronic volume register |
| Electronic volume register set | 0 | 1 | 0 | * | * | Electronic volume value | | | | | | |

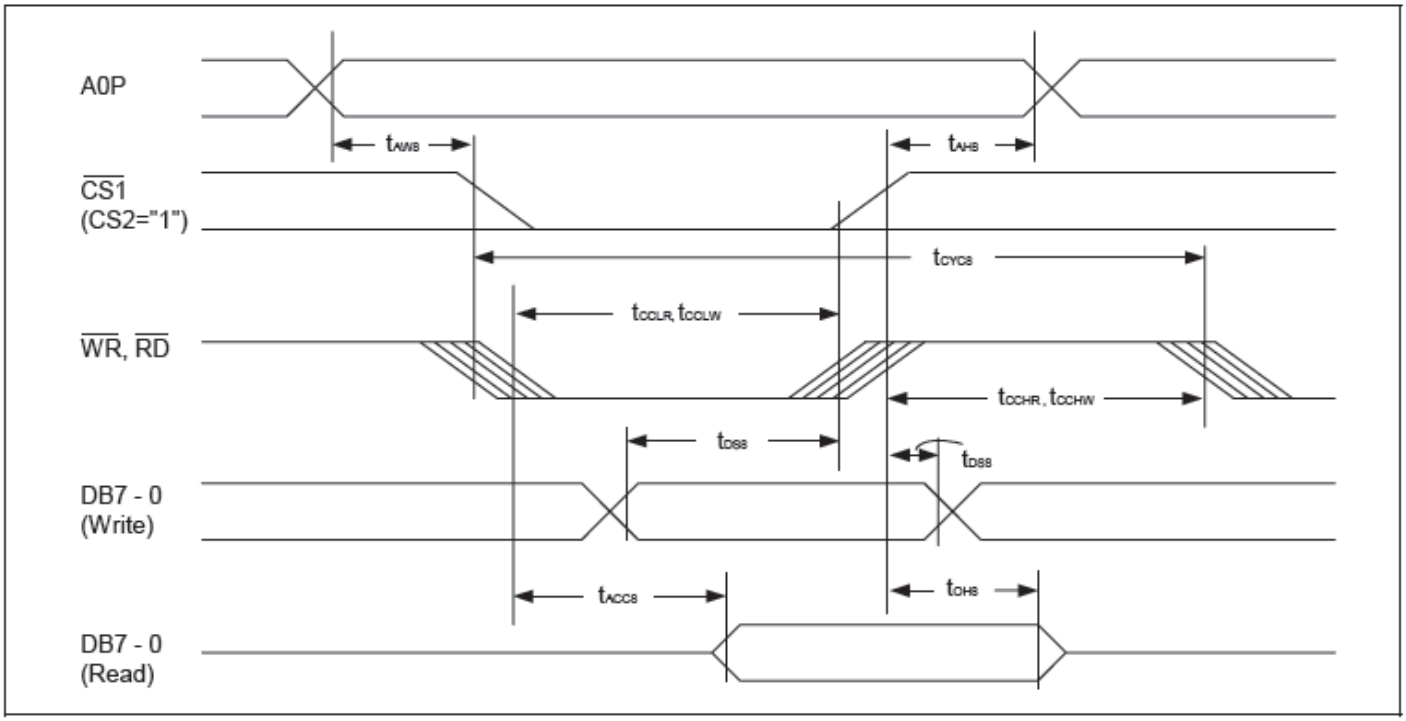
| Command | Command Code | | | | | | | | | | Function |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | A0P | $\overline{RD}$ | $\overline{WR}$ | DB7 | DB6 | DB5 | DB4 | DB3 | DB2 | DB1 | DB0 | |
| 19). Static indicator ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0: OFF, 1: ON |
| | | | | | | | | | | | 1 | |
| Static indicator Register set | | | | * | * | * | * | * | * | Mode | | Set the flashing mode |
| 20). Page Blink | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | |
| Page selection | 0 | 1 | 0 | P7 | P6 | P5 | P4 | P3 | P2 | P1 | P0 | P7 - 0: 1 - blinking page 0 - no blinking, normal display |
| 21). Driving Mode Set | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | Set the driving mode register |
| Mode selection | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | D0 | Driving capability (D0): (1)>(0) |
| 22). Power saver | | | | | | | | | | | | Display OFF and display all points ON compound command |
| 23). NOP | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | Command for non-operation |
| 24). Test | 0 | 1 | 0 | 1 | 1 | 1 | 1 | * | * | * | * | Command for IC test. Do not use this command |
| | | | | 1 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | |
| 25). Oscillator Frequency selection | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 20KHz/33KHz (Default) |
| | | | | | | | | | | | 1 | 16.4KHz/ 27.06KHz |

## DISPLAY DATA RAM



# TIMING CHARACTERISTICS

**System bus read/write characteristics 1 (For the 8080 Series MPU)**




(VDD = 3.3V to 3.6V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0P | $t_{AH8}$ | | 0 | - | ns |
| Address setup time | | $t_{AW8}$ | | 0 | - | ns |
| System cycle time | A0P | $t_{CYC8}$ | | 240 | - | ns |
| Control L pulse width ( $\overline{WR}$ ) | $\overline{WR}$ | $t_{CCLW}$ | | 80 | - | ns |
| Control L pulse width ( $\overline{RD}$ ) | $\overline{RD}$ | $t_{CCLR}$ | | 80 | - | ns |
| Control H pulse width ( $\overline{WR}$ ) | $\overline{WR}$ | $t_{CCHW}$ | | 80 | - | ns |
| Control H pulse width ( $\overline{RD}$ ) | $\overline{RD}$ | $t_{CCHR}$ | | 80 | - | ns |
| Data setup time | DB7 - 0 | $t_{DS8}$ | | 30 | - | ns |
| Address hold time | | $t_{DH8}$ | | 10 | - | ns |
| $\overline{RD}$ access time | | $t_{ACC8}$ | $C_L$ = 100pF | - | 70 | ns |
| Output disable time | | $t_{OH8}$ | | 5.0 | 50 | ns |

(VDD = 2.7V to 3.3V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0P | $t_{AH8}$ | | 0 | - | ns |
| Address setup time | | $t_{AW8}$ | | 0 | - | ns |
| System cycle time | A0P | $t_{CYC8}$ | | 400 | - | ns |
| Control L pulse width ( $\overline{WR}$ ) | $\overline{WR}$ | $t_{CCLW}$ | | 100 | - | ns |
| Control L pulse width ( $\overline{RD}$ ) | $\overline{RD}$ | $t_{CCLR}$ | | 100 | - | ns |
| Control H pulse width ( $\overline{WR}$ ) | $\overline{WR}$ | $t_{CCHW}$ | | 100 | - | ns |
| Control H pulse width ( $\overline{RD}$ ) | $\overline{RD}$ | $t_{CCHR}$ | | 100 | - | ns |
| Data setup time | DB7 - 0 | $t_{DS8}$ | | 40 | - | ns |
| Address hold time | | $t_{DH8}$ | | 15 | - | ns |
| $\overline{RD}$ access time | | $t_{ACC8}$ | $C_L$ = 100pF | - | 140 | ns |
| Output disable time | | $t_{OH8}$ | | 10 | 100 | ns |

(VDD = 1.8V to 2.7V, $T_A$ = -20 to 75℃)

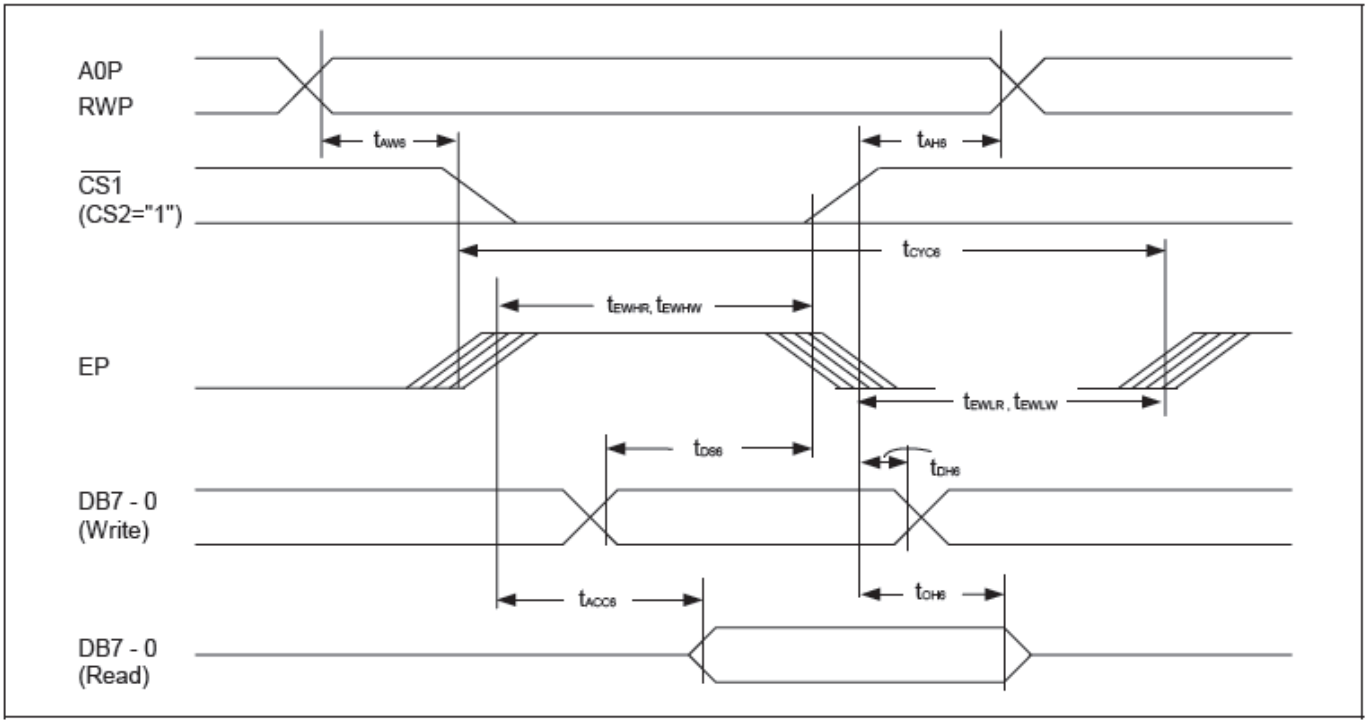
| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Address hold time | A0P | $t_{AH8}$ | | 0 | - | ns |
| Address setup time | | $t_{AW8}$ | | 0 | - | ns |
| System cycle time | A0P | $t_{CYC8}$ | | 640 | - | ns |
| Control L pulse width ( $\overline{WR}$ ) | $\overline{WR}$ | $t_{CCLW}$ | | 200 | - | ns |
| Control L pulse width ( $\overline{RD}$ ) | $\overline{RD}$ | $t_{CCLR}$ | | 200 | - | ns |
| Control H pulse width ( $\overline{WR}$ ) | $\overline{WR}$ | $t_{CCHW}$ | | 200 | - | ns |
| Control H pulse width ( $\overline{RD}$ ) | $\overline{RD}$ | $t_{CCHR}$ | | 200 | - | ns |
| Data setup time | DB7 - 0 | $t_{DS8}$ | | 80 | - | ns |
| Address hold time | | $t_{DH8}$ | | 30 | - | ns |
| $\overline{RD}$ access time | | $t_{ACC8}$ | $C_L$ = 100pF | - | 280 | ns |
| Output disable time | | $t_{OH8}$ | | 10 | 200 | ns |

**Note1:** The input signal rise time and fall time ($t_r$, $t_f$) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC8} - t_{CCLW} - t_{CCHW})$ for $(t_r + t_f) \leqq (t_{CYC8} - t_{CCLR} - t_{CCHR})$ are specified.

**Note2:** All timing is specified using 20% and 80% of VDD as the reference.

**Note3:** $t_{CCLW}$ and $t_{CCLR}$ are specified as the overlap between CS1 being 'L' ( CS2 = 'H') and $\overline{WR}$ and $\overline{RD}$ being at the 'L' level.

**System bus read/write characteristics 2 (6800 series MPU)**




(VDD = **3.3V to 3.6V,** $T_A$ = -20 to 75℃)

| Item | | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| Address hold time | | A0P | $t_{AH6}$ | | 0 | - | ns |
| Address setup time | | | $t_{AW6}$ | | 0 | - | ns |
| System cycle time | | A0P | $t_{CYC6}$ | | **240** | - | ns |
| Data setup time | | DB7 - 0 | $t_{DS6}$ | $C_L$ = 100pF | 30 | - | ns |
| Data hold time | | | $t_{DH6}$ | | 10 | - | ns |
| Access time | | | $t_{ACC6}$ | | - | 70 | ns |
| Output disable time | | | $t_{OH6}$ | | 10 | 50 | ns |
| Enable H pulse time | Read | EP | $t_{EWHR}$ | | 80 | - | ns |
| | Write | | $t_{EWHW}$ | | 80 | - | ns |
| Enable L pulse time | Read | EP | $t_{EWLR}$ | | 80 | - | ns |
| | Write | | $t_{EWLW}$ | | 80 | - | ns |

(VDD = 2.7V to 3.3V, $T_A$ = -20 to 75℃)

| Item | | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| Address hold time | | A0P | $t_{AH6}$ | | 0 | - | ns |
| Address setup time | | | $t_{AW6}$ | | 0 | - | ns |
| System cycle time | | A0P | $t_{CYC6}$ | | 400 | - | ns |
| Data setup time | | DB7 - 0 | $t_{DS6}$ | $C_L$ = 100pF | 40 | - | ns |
| Data hold time | | | $t_{DH6}$ | | 15 | - | ns |
| Access time | | | $t_{ACC6}$ | | - | 140 | ns |
| Output disable time | | | $t_{OH6}$ | | 10 | 100 | ns |
| Enable H pulse time | Read | EP | $t_{EWHR}$ | | 100 | - | ns |
| | Write | | $t_{EWHW}$ | | 100 | - | ns |
| Enable L pulse time | Read | EP | $t_{EWLR}$ | | 100 | - | ns |
| | Write | | $t_{EWLW}$ | | 100 | - | ns |

(VDD = 1.8V to 2.7V, $T_A$ = -20 to 75℃)

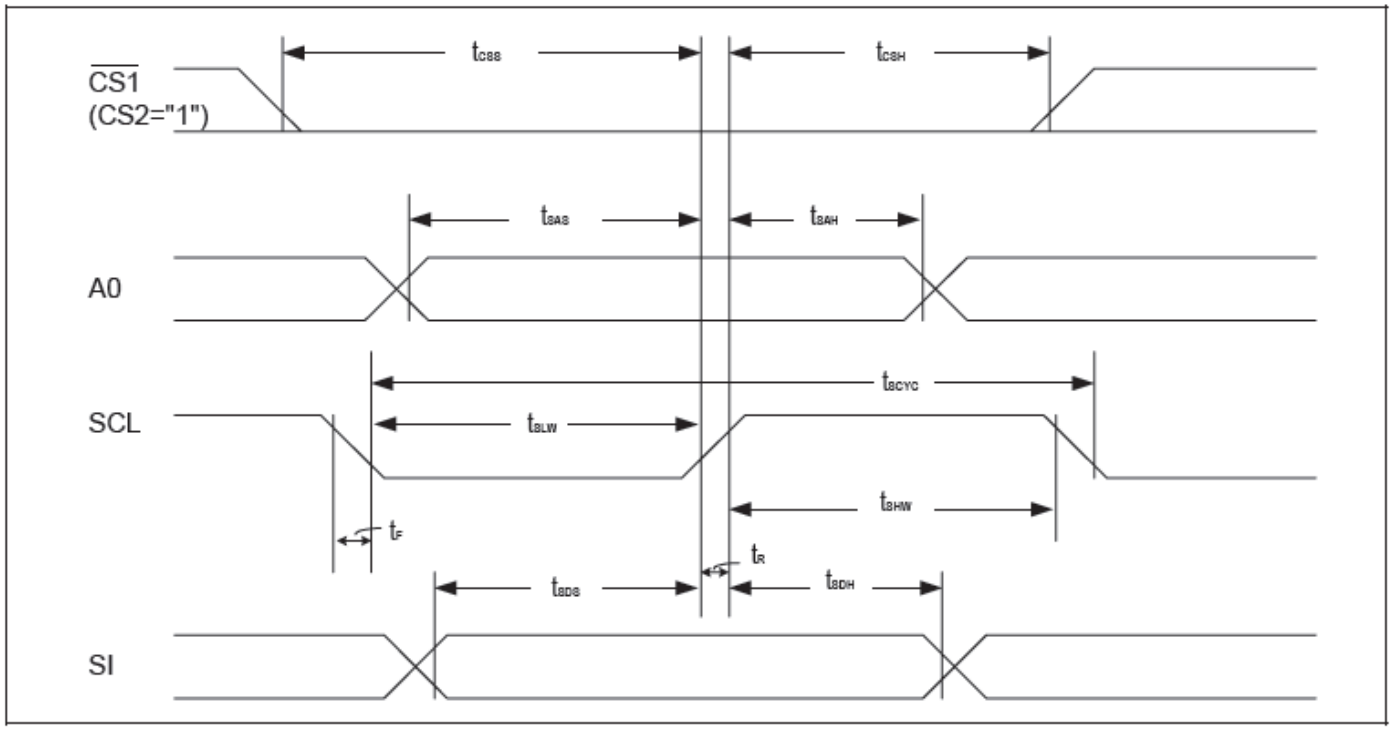
| Item | | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|---|
| | | | | | Min. | Max. | |
| Address hold time | | A0P | $t_{AH6}$ | | 0 | - | ns |
| Address setup time | | | $t_{AW6}$ | | 0 | - | ns |
| System cycle time | | A0P | $t_{CYC6}$ | | 640 | - | ns |
| Data setup time | | DB7 - 0 | $t_{DS6}$ | $C_L$ = 100pF | 80 | - | ns |
| Data hold time | | | $t_{DH6}$ | | 30 | - | ns |
| Access time | | | $t_{ACC6}$ | | - | 280 | ns |
| Output disable time | | | $t_{OH6}$ | | 10 | 120 | ns |
| Enable H pulse time | Read | EP | $t_{EWHR}$ | | 200 | - | ns |
| | Write | | $t_{EWHW}$ | | 200 | - | ns |
| Enable L pulse time | Read | EP | $t_{EWLR}$ | | 200 | - | ns |
| | Write | | $t_{EWLW}$ | | 200 | - | ns |

**Note1:** The input signal rise time and fall time (tr, tf) is specified at 15 ns or less. When the system cycle time is extremely fast, $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLW} - t_{EWHW})$ for $(t_r + t_f) \leqq (t_{CYC6} - t_{EWLR} - t_{EWHR})$ are specified.

**Note2:** All timing is specified using 20% and 80% of VDD as the reference.

**Note3:** $t_{EWLW}$ and $t_{EWLR}$ are specified as the overlap between $\overline{CS1}$ being 'L' (CS2 = 'H') and EP.

# THE SERIAL INTERFACE




(VDD = 3.3V to 3.6V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Serial Clock Period | SCL | $t_{SCYC}$ | - | 200 | - | ns |
| SCL 'H' pulse width | | $t_{SHW}$ | - | 80 | - | ns |
| SCL 'L' pulse width | | $t_{SLW}$ | - | 80 | - | ns |
| Address setup time | A0P | $t_{SAS}$ | - | 50 | - | ns |
| Address hold time | | $t_{SAH}$ | - | 100 | - | ns |
| Data setup time | SI | $t_{SDS}$ | - | 50 | - | ns |
| Data hold time | | $t_{SDH}$ | - | 50 | - | ns |
| CS-SCL time | CS | $t_{CSS}$ | - | 100 | - | ns |
| | | $t_{CSH}$ | - | 100 | - | ns |

(VDD = 2.7V to 3.3V, $T_A$ = -20 to 75℃)

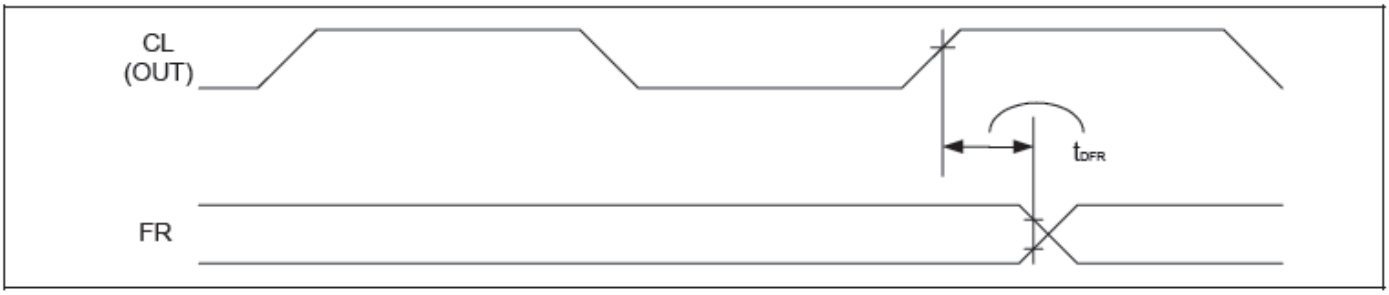
| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Serial Clock Period | SCL | tSCYC | - | 250 | - | ns |
| SCL 'H' pulse width | | tSHW | - | 100 | - | ns |
| SCL 'L' pulse width | | tSLW | - | 100 | - | ns |
| Address setup time | A0P | tSAS | - | 150 | - | ns |
| Address hold time | | tSAH | - | 150 | - | ns |
| Data setup time | SI | tSDS | - | 100 | - | ns |
| Data hold time | | tSDH | - | 100 | - | ns |
| CS-SCL time | CS | tCSS | - | 150 | - | ns |
| | | tCSH | - | 150 | - | ns |

| Item | Signal | Symbol | Condition | Rating | | Units |
|---|---|---|---|---|---|---|
| | | | | Min. | Max. | |
| Serial Clock Period | SCL | $t_{SCYC}$ | - | 350 | - | ns |
| SCL 'H' pulse width | | $t_{SHW}$ | - | 150 | - | ns |
| SCL 'L' pulse width | | $t_{SLW}$ | - | 150 | - | ns |
| Address setup time | A0P | $t_{SAS}$ | - | 150 | - | ns |
| Address hold time | | $t_{SAH}$ | - | 150 | - | ns |
| Data setup time | SI | $t_{SDS}$ | - | 60 | - | ns |
| Data hold time | | $t_{SDH}$ | - | 30 | - | ns |
| CS-SCL time | CS | $t_{CSS}$ | - | 250 | - | ns |
| | | $t_{CSH}$ | - | 250 | - | ns |

**Note1:** The input signal rise and fall time ($t_r$, $t_f$) are specified at 15 ns or less.

**Note2:** All timing is specified using 20% and 80% of VDD as the standard.

## DISPLAY CONTROL OUTPUT TIMING




(VDD = 3.3V to 3.6V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| FR delay time | FR | $t_{DFR}$ | $C_L$ = 50pF | - | 10 | 40 | ns |

(VDD = 2.7V to 3.3V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| FR delay time | FR | $t_{DFR}$ | $C_L$ = 50pF | - | 20 | 80 | ns |

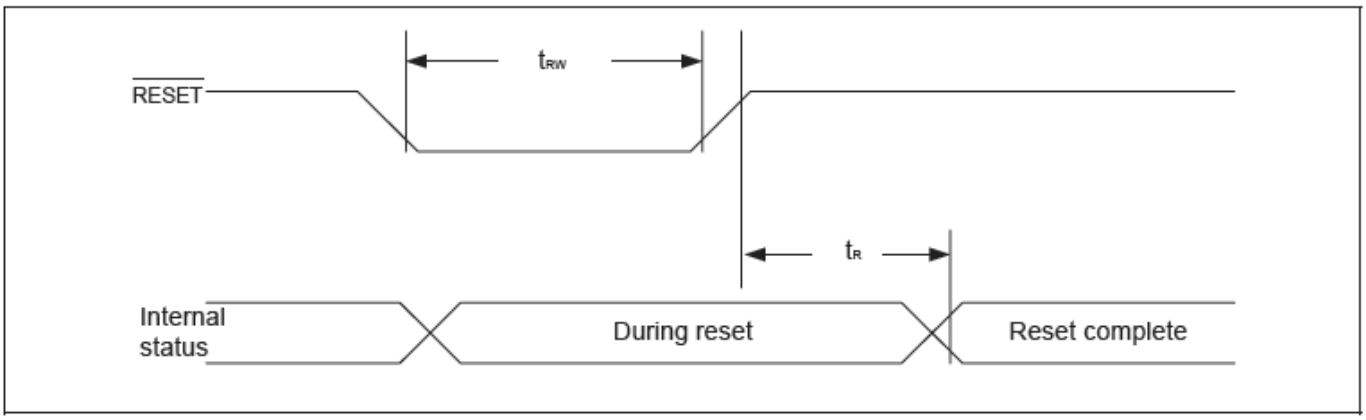
(VDD = 1.8V to 2.7V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| FR delay time | FR | $t_{DFR}$ | $C_L$ = 50pF | - | 50 | 200 | ns |

**Note1:** Valid only when the master mode is selected.

**Note2:** All timing is based on 20% and 80% of VDD.

# RESET TIMING




(VDD = 3.3 V to 3.6V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Reset time | | $t_R$ | - | - | - | 0.5 | μs |
| Reset 'L' pulse width | RES | $t_{RW}$ | | 0.5 | - | - | μs |

(VDD = 2.7V to 3.3V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Reset time | | $t_R$ | - | - | - | 1.0 | μs |
| Reset 'L' pulse width | RES | $t_{RW}$ | | 1.0 | - | - | μs |

(VDD = 1.8V to 2.7V, $T_A$ = -20 to 75℃)

| Item | Signal | Symbol | Condition | Rating | | | Units |
|---|---|---|---|---|---|---|---|
| | | | | Min. | Typ. | Max. | |
| Reset time | | $t_R$ | - | - | - | 1.5 | μs |
| Reset 'L' pulse width | RES | t | | 1.5 | - | - | μs |

**Note:** All timing is specified with 20% and 80% of VDD as the standard.

# ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = VOP / 64 Hz
TEMPERATURE = 22 ± 5 ℃
RELATIVE HUMIDITY = 60 ± 15 %

| ITEM | SYMBOL | UNIT | TYP. STN |
|---|---|---|---|
| RESPONSE TIME | Ton | ms | 220 |
| | Toff | ms | 280 |
| CONTRAST RATIO | Cr | - | 12 |
| VIEWING ANGLE (Cr ≥ 2) | V3:00 | ° | 40 |
| | V6:00 | ° | 70 |
| | V9:00 | ° | 40 |
| | V12:00 | ° | 50 |

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

# RELIABILITY OF LCD MODULE

| ITEM | TEST CONDITION FOR NORMAL TEMPERATURE | TEST CONDITION FOR WIDE TEMPERATURE | TIME |
|---|---|---|---|
| High temperature operating | 50°C | 70°C | 240 hours |
| Low temperature operating | 0°C | -20°C | 240 hours |
| High temperature storage | 60°C | 80°C | 240 hours |
| Low temperature storage | -10°C | -30°C | 240 hours |
| Temperature-humidity storage | 40°C 90% R.H. | 60°C 90% R.H. | 96 hours |
| Temperature cycling | -10°C to 60°C<br>30 Min Dwell | -30°C to 80°C<br>30 Min Dwell | 5 cycle |
| Vibration Test at LCM Level | Freq 10-55 Hz<br>Sweep rate: 10-55-10 at 1 min<br>Sweep mode Linear<br>Displacement: 2 mm p-p<br>1 Hour each for X, Y, Z | Freq 10-55 Hz<br>Sweep rate: 10-55-10 at 1 min<br>Sweep mode Linear<br>Displacement: 2 mm p-p<br>1 Hour each for X, Y, Z | — |

## SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65 MINOR – 1.5

## QUALITY STANDARD

| DEFECT | CRITERIA | TYPE | FIGURE |
|---|---|---|---|
| SHORT CIRCUIT | - | MAJOR | - |
| MISSING SEGMENT | - | MAJOR | - |
| UNEVEN / POOR CONTRAST | - | MAJOR | - |
| CROSS TALK | - | MAJOR | - |
| PIN HOLE | MAX(a,b) ≤ 1 / 4 W | MINOR | 1 |
| EXCESS SEGMENT | MAX(c,d) ≤ 1 / 4 T | MINOR | 1 |
| BUBBLES | d* ≥ 0.2 QTY=0 | MINOR | 2 |
| BLACKS SPOTS | d ≤ 0.3 N.A.**<br>0.3<d≤0.4 QTY≤1<br>0.4<d QTY=0 | MINOR | 2 |
| LINE SCRATCHES | x≥0.7 y≥0.05 QTY=0 | MINOR | 3 |
| BLACK LINE | x≥0.7 y≥0.05 QTY=0 | MINOR | 3 |

*d = MAX ($d_1$,$d_2$) ** N. A . = NOT APPLICABLE DEFECT TABLE : B

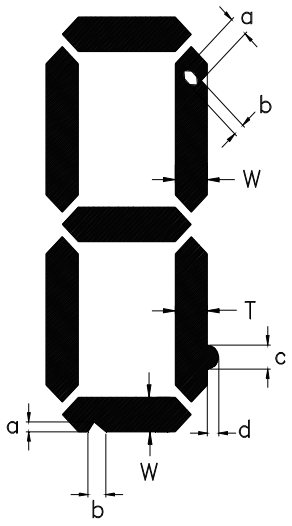
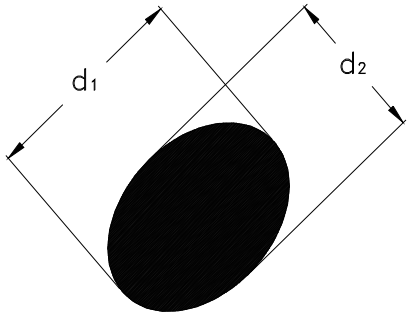
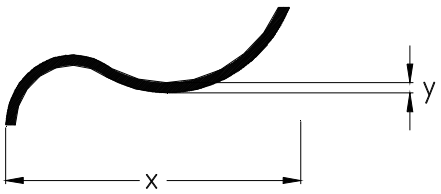



fig . 1




POLARIZER BUBBLES / SPOTS
fig . 2




LINE SCRATCHES / BLACK LINE
fig . 3

# QUALITY STANDARD ( CONT .)

| DEFECT | | CRITERIA | TYPE | FIGURE |
|---|---|---|---|---|
| CHIPS | CONTACT EDGE | e≤1/2T f≤1/3W g≤3.5 | MINOR | 4 |
| | BOTTOM GLASS | p≤1.0 q≤3.5 r≤1/2T | | 4 |
| | CORNER | a≤1.5 b≤W | | 4 |
| | TOP GLASS | a≤3.0 b≤1/3T c≤1/2W | | 5 |
| GLASS PROTRUSION | | a ≤ 1/4 W | MINOR | 6 |
| RAINBOW | | - | MINOR | - |

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : B

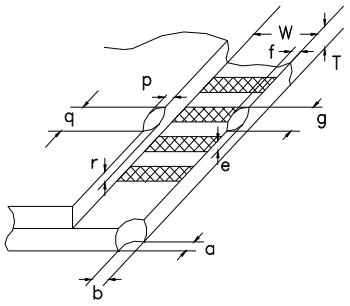



fig . 4

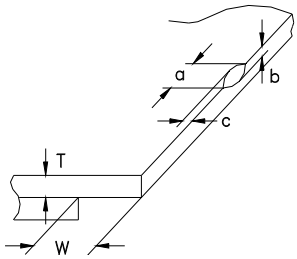



fig . 5

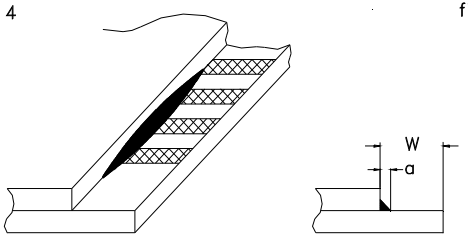



fig . 6

# HANDLING PRECAUTIONS

## (1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly.
- Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent;
-water, ketone, aromatics

## (2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to $V_{DD}$ or $V_{SS}$, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

Remove the protective film slowly and, if possible, under ESD control device like ion blower and humidity of working room should be kept over 50%RH to reduce risk of static charge.

## (3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

## (4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

## (5) SOLDERING (for Pin type)

It is recommended to complete dip soldering at 270 $^{o}$C or hand soldering at 280 $^{o}$C within 3 seconds. The soldering position is at least 3mm apart from the pin head. Wave or reflow soldering are not recommended. Metal pins should not be soldered for more than 3 times and each soldering should be done after cool down of metal pins**.**

## (6) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

## WARRANTY

CLOVER CHINA will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of CLOVER CHINA is limited to repair and/or replacement. CLOVER CHINA will not be responsible for any subsequent or consequential event.