CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model : CG9616A - _ _ - _ _ - _ _ - _

Revision	00
Engineering	Timothy Chan
Date	05 JUL 2021
Our Reference	X9066K

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(Can be omitted if not used)
T – Touch panel (Analog)
P – Touch panel (Digital)

MODE OF DISPLAY

Display mode	**Display condition**	**Viewing direction**
STN : ☐ Yellow green	☐ Reflective type	☐ 6 O' clock
☐ Grey	☐ Transflective type	☐ 12 O' clock
☐ Blue (negative)	☐ Transmissive type	☐ 3 O' clock
☐ FSTN positive	☐ Others	☐ 9 O' clock
☐ FSTN negative		

LCD MODULE NUMBER NOTATION:

CG9616A- N N - S R - N 6 – T
(1) (2) (3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
T – TN
V – TN (Negative)
S – STN Yellow green
G – STN Grey
B – STN Blue (Negative)
F – FSTN
N – FSTN (Negative)
*(5)---Rear polarizer type
R – Reflective
F – Transflective
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)

GENERAL DESCRIPTION

Display mode	:	96 X 16 dots, Graphic COG LCD module
	:	FSTN / Negative / Reflective
Interface	:	I2C
Driving method	:	1/16 duty, 1/6 bias
Controller IC	:	Sitronix ST7539i-G4 or equivalent For the detailed information, please refer to the IC specifications.

MECHANICAL DIMENSIONS

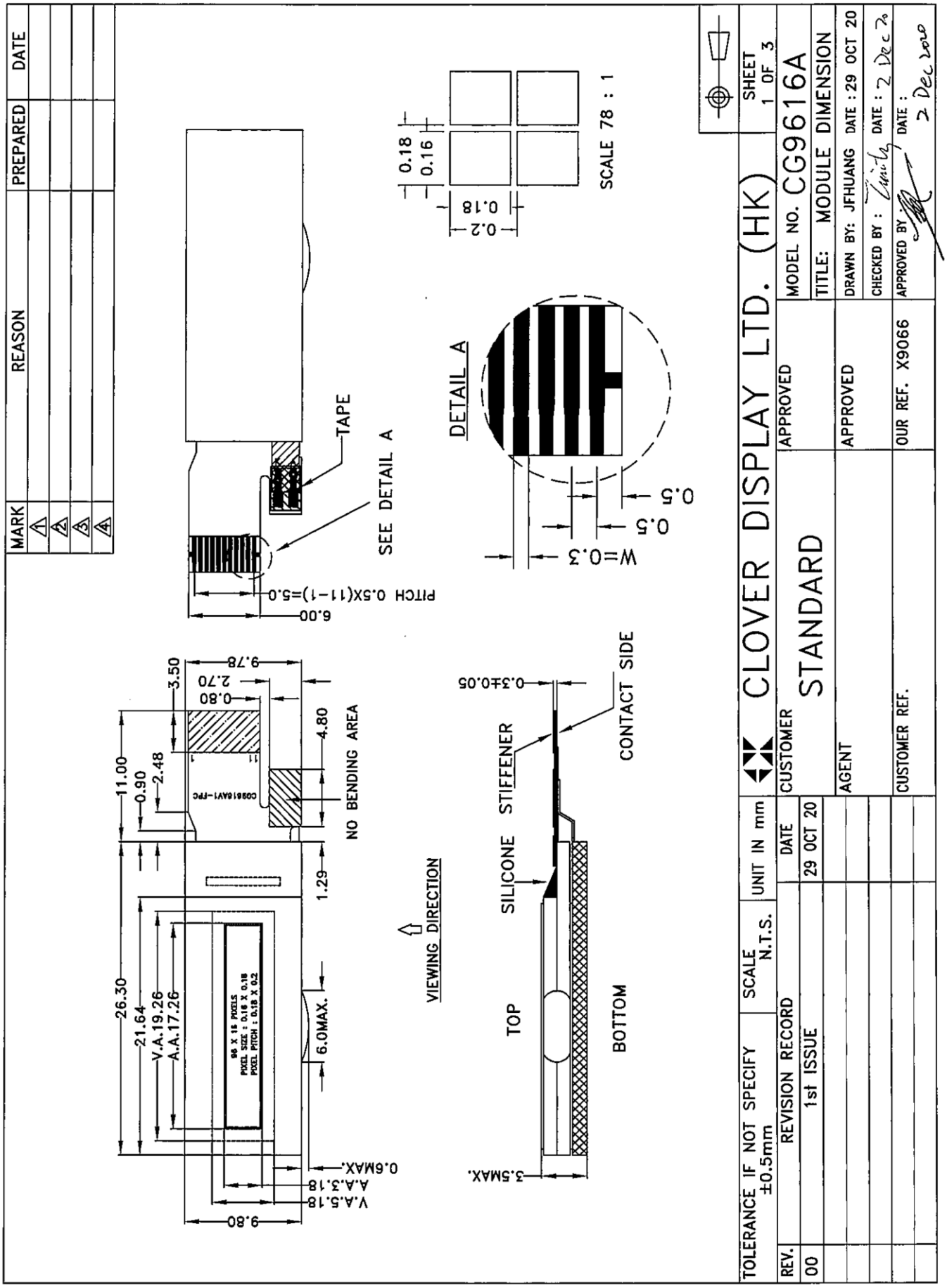
Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension	26.3(L)x9.8(W)x2.1 (H)	mm	Dot Pitch	0.18(L)x0.2(W)	mm
Viewing Area	19.26(L)x5.18(W)	mm	Dot Size	0.16(L)x0.18(W)	mm
Active Area	17.26(L)x3.18(W)	mm			

CONNECTOR PIN ASSIGNMENT

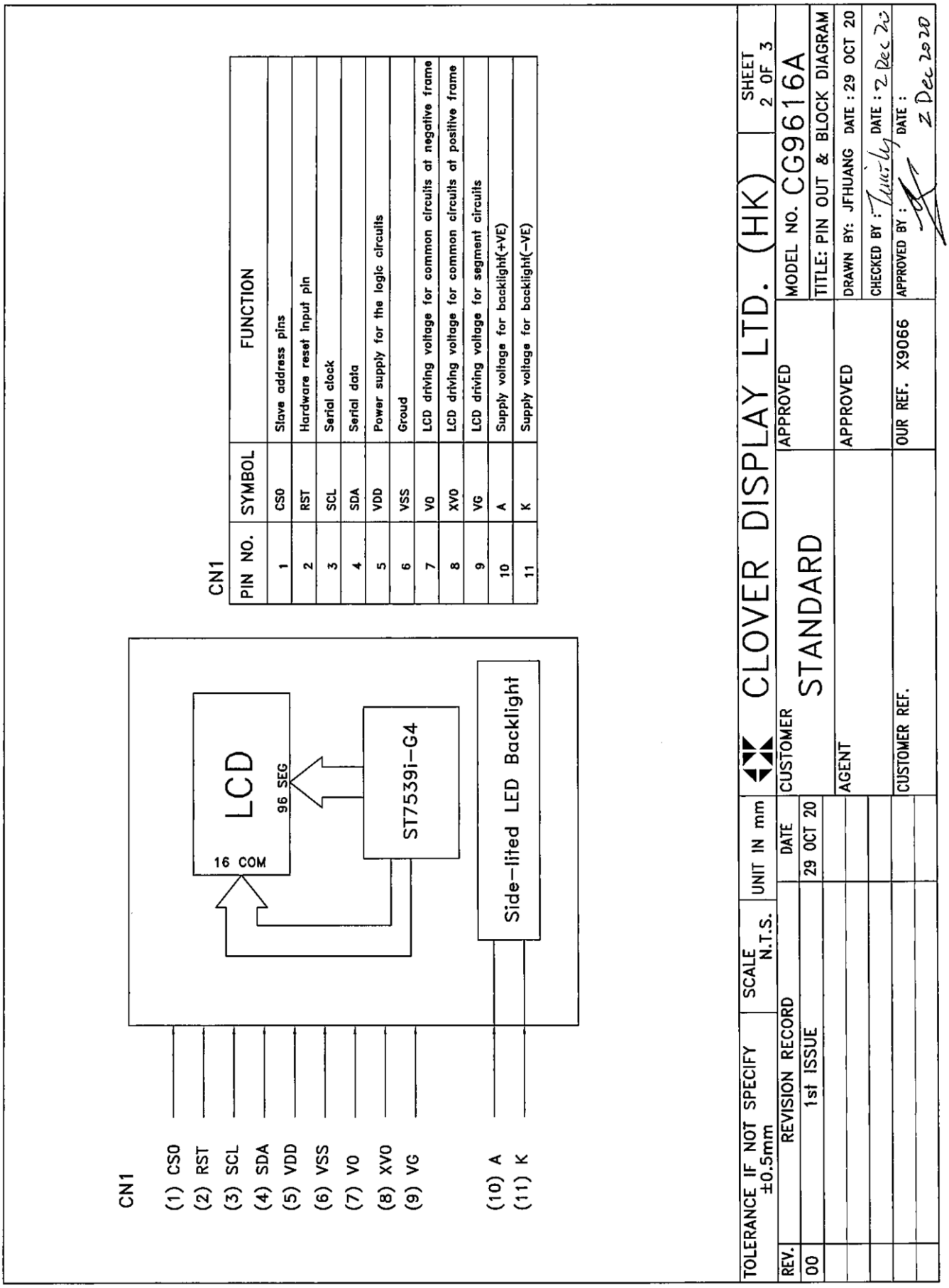
Pin No.	Symbol	Function
1	CS0	Slave address pins
2	RST	Hardware reset input pin
3	SCL	Serial clock
4	SDA	Serial data
5	VDD	Power supply for the logic circuits
6	VSS	Groud
7	V0	LCD driving voltage for common circuits at negative frame
8	XV0	LCD driving voltage for common circuits at negative frame
9	VG	LCD driving voltage for segment circuits
*10	A	Supply Voltage for Backlight (+VE)
*11	K	Supply Voltage for Backlight (-VE)

Note (*) : Pin 10, 11 are used for backlight version

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage for Logic	VDD	3.05	3.3	3.55	V
Supply Current for Logic	IDD	–	0.15	0.23	mA
Operating Voltage for LCD	VLCD	–	7	–	V
'High' Level Input Voltage	VIH	0.8VDD	–	–	V
'Low' Level Input Voltage	VIL	–	–	0.2VDD	V

Note (*): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Side BL:

Constant voltage driving:

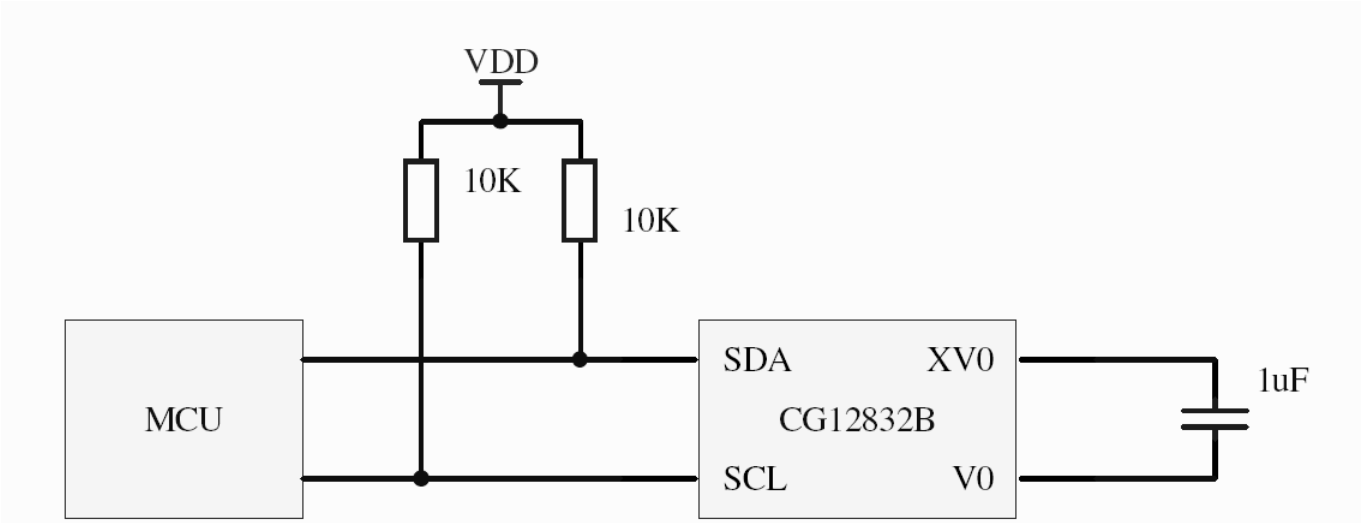
Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Backlight current	I_{BL}	–		20	mA	V_{BL} = 3.3V

ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage	VDD	-0.3 to 4.0	-0.3 to 4.0	V
Input Voltage	Vi	-0.3 to VDD+0.3	-0.3 to VDD+0.3	V
Operating Temperature	Topr	-20 to 70	-40 to 90	℃
Storage Temperature	Tstg	-30 to 80	-50 to 100	℃

REFERENCE CIRCUIT EXAMPLE



INSTRUCTIONS TABLE

COMMAND TABLE											
INSTRUCTION	A0	R/W (RWR)	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
Write Data	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data to DDRAM
Read Data	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from DDRAM Only for parallel interface and I^2C
Read Status Byte (parallel interface)	0	1	ID0	MX	MY	WA	DE	0	0	0	Read status byte Only for parallel interface
			0	POR	0	0	0	ID3	ID2	ID1	
Read Status Byte (4-SPI)	0	0	1	1	1	1	1	1	1	0	Read status byte Only for 4 line SPI
	0	1	ID0	MX	MY	WA	DE	0	0	0	
			0	POR	0	0	0	ID3	ID2	ID1	
Set Column Address LSB	0	0	0	0	0	0	CA3	CA2	CA1	CA0	Set column address of RAM
Set Column Address MSB	0	0	0	0	0	1	CA7	CA6	CA5	CA4	
Set Scroll Line	0	0	0	1	SL5	SL4	SL3	SL2	SL1	SL0	Specify line address for the 1st display line of DDRAM (vertical scrolling)
Set Page Address	0	0	1	0	1	1	PA3	PA2	PA1	PA0	Set page address of RAM
Set Contrast	0	0	1	0	0	0	0	0	0	1	2-byte instruction. Set Vop voltage
			EV7	EV6	EV5	EV4	EV3	EV2	EV1	EV0	
Set Partial Screen Mode	0	0	1	0	0	0	0	1	0	PS	PS=1: Enable partial mode
Set RAM Address Control	0	0	1	0	0	0	1	AC2	AC1	AC0	Set column and page address behavior
Set Frame Rate	0	0	1	0	1	0	0	0	FR1	FR0	Set frame frequency
Set All Pixel ON	0	0	1	0	1	0	0	1	0	AP	Set all display segments on
Set Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display
Set Display Enable	0	0	1	0	1	0	1	1	1	PD	PD=0: Chip is in power down mode
Scan Direction	0	0	1	1	0	0	0	MY	MX	0	Set COM and SEG scan direction
Software Reset	0	0	1	1	1	0	0	0	1	0	Set software reset
NOP	0	0	1	1	1	0	0	0	1	1	No operation
Set Bias	0	0	1	1	1	0	1	0	BR1	BR0	Set internal bias circuit
Set COM End	0	0	1	1	1	1	0	0	0	1	2-byte instruction. Set display duty
			--	--	CEN5	CEN4	CEN3	CEN2	CEN1	CEN0	
Partial Start Address	0	0	1	1	1	1	0	0	1	0	Set partial start for partial display screen
			--	--	DST5	DST 4	DST 3	DST 2	DST 1	DST 0	
Partial End Address	0	0	1	1	1	1	0	0	1	1	Set partial end for partial display screen
			--	--	DEN5	DEN4	DEN3	DEN2	DEN1	DEN0	
Test Control	0	0	1	1	1	1	1	1	1	1	Set test command table
			--	--	--	--	--	--	H1	H0	

Note: 1. Do not use instructions not listed in these tables (Command Table).

2. "--" = Disabled bit. It can be either logic 0 or 1.

RECOMMENDED INITIAL SETTINGS

Set Page Address : B0H
Set Column Address:10H,00H
Set Scan Direction:C2H
Set RAM Address Control:88H
Set LCD Bias Select:E8H
Set LCD Duty Select : F1H,0FH
Set Scroll Line:40H
Set Frame Rate:A0H
Set Electronic volume register:81H,A9H
Set Display On : AFH

DISPLAY DATA RAM

When accessing to RAM, sixteen addressing mode are provided:

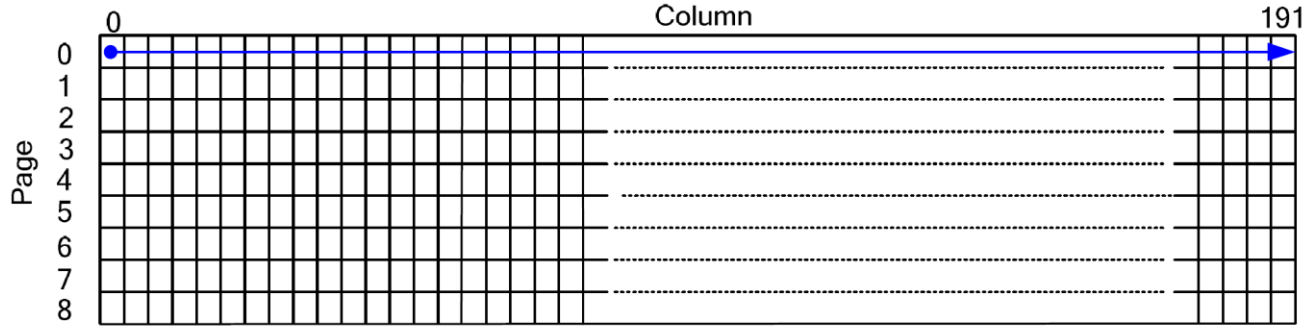


Fig 12. DDRAM Access Mapping (MX=0, AC[2:0]=0, PA[3:0]=0, CA[3:0]=0)

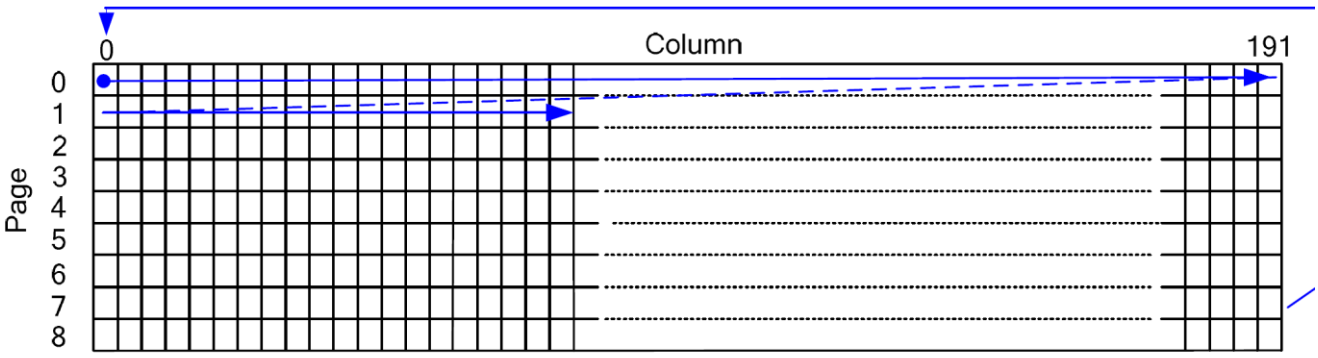


Fig 13. DDRAM Access Mapping (MX=0, AC[2:0]=1, PA[3:0]=0, CA[3:0]=0)

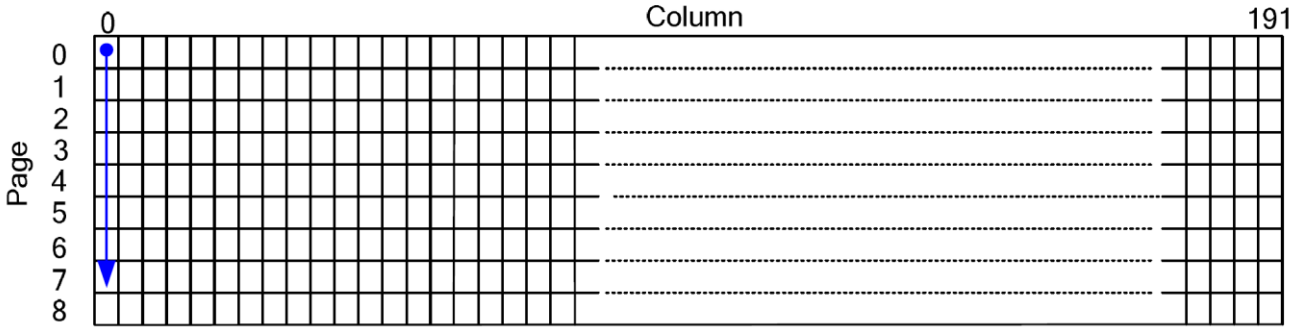


Fig 14. DDRAM Access Mapping (MX=0, AC[2:0]=2, PA[3:0]=0, CA[3:0]=0)

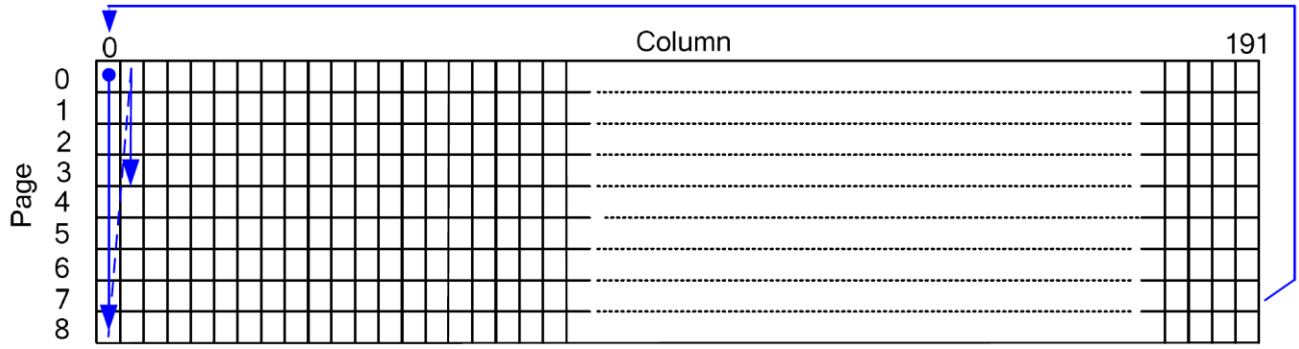


Fig 15. DDRAM Access Mapping (MX=0, AC[2:0]=3, PA[3:0]=0, CA[3:0]=0)

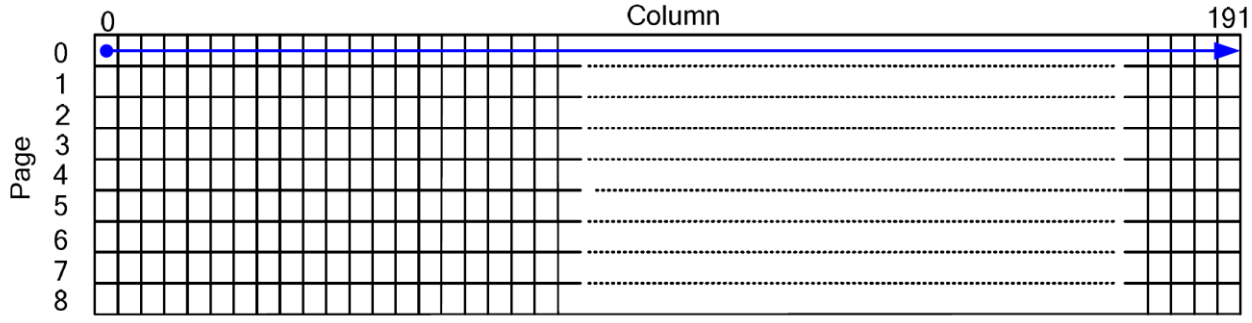


Fig 16. DDRAM Access Mapping (MX=0, AC[2:0]=4, PA[3:0]=0, CA[3:0]=0)

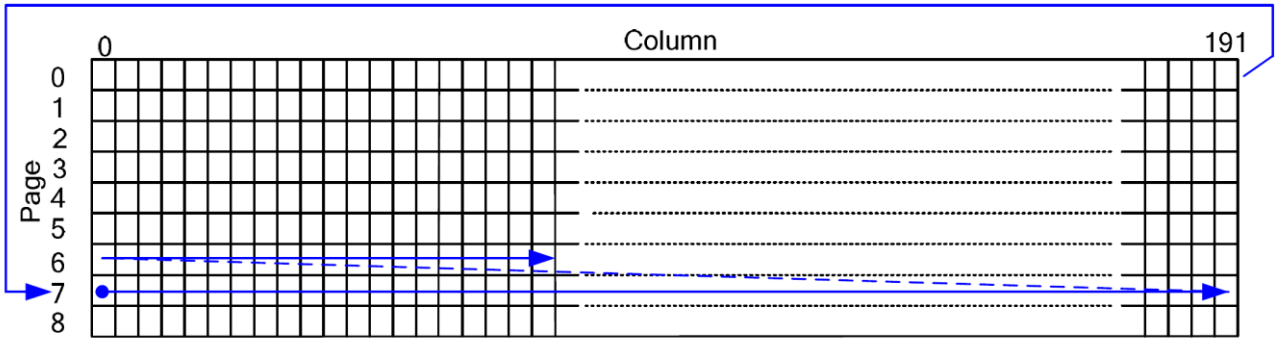


Fig 17. DDRAM Access Mapping (MX=0, AC[2:0]=5, PA[3:0]=7, CA[3:0]=0)

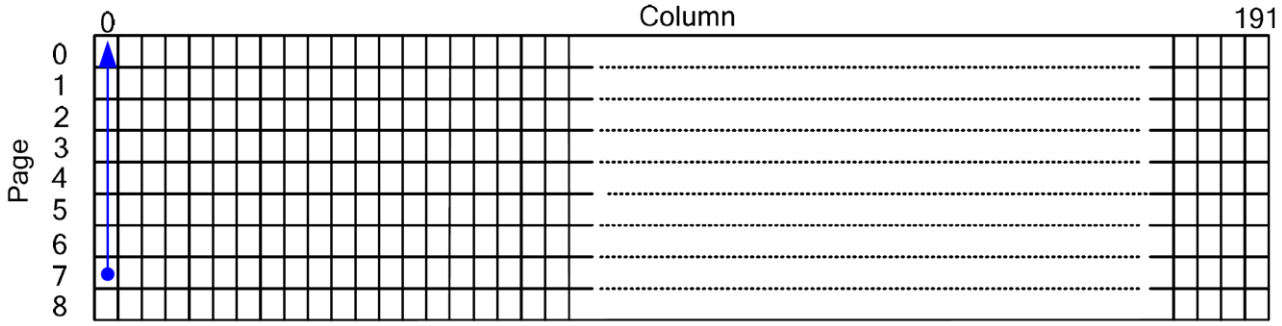


Fig 18. DDRAM Access Mapping (MX=0, AC[2:0]=6, PA[3:0]=7, CA[3:0]=0)

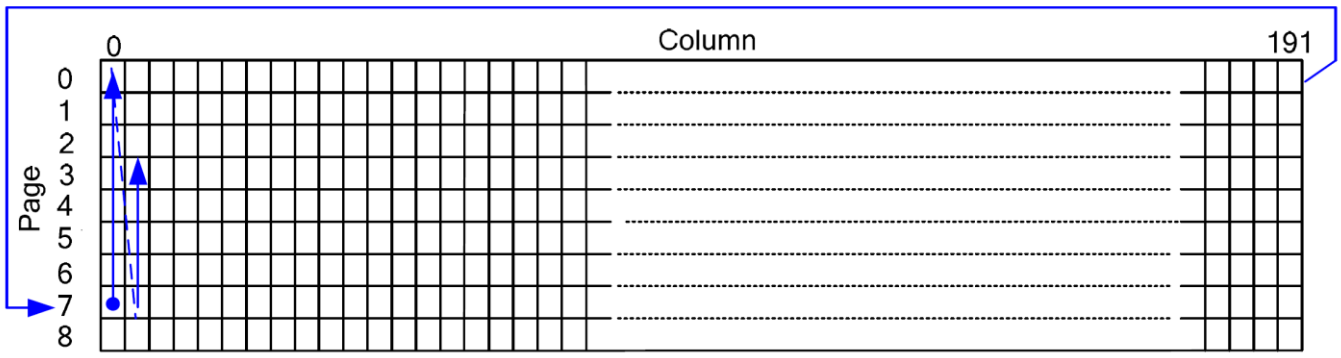


Fig 19. DDRAM Access Mapping (MX=0, AC[2:0]=7, PA[3:0]=7, CA[3:0]=0)

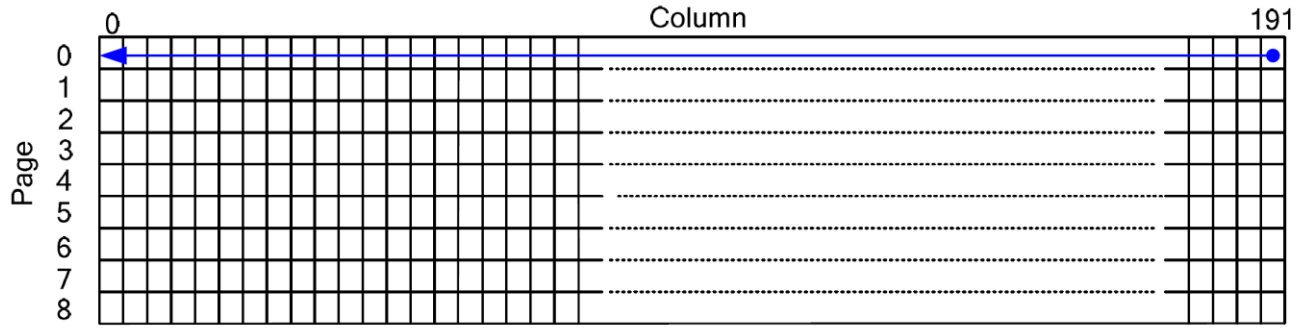


Fig 20. DDRAM Access Mapping (MX=1, AC[2:0]=0, PA[3:0]=0, CA[3:0]=0)

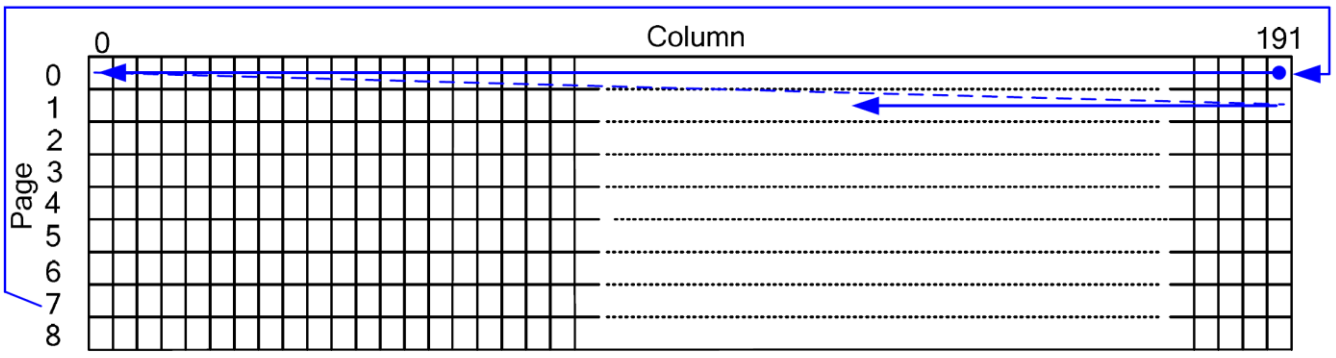


Fig 21. DDRAM Access Mapping (MX=1, AC[2:0]=1, PA[3:0]=0, CA[3:0]=0)

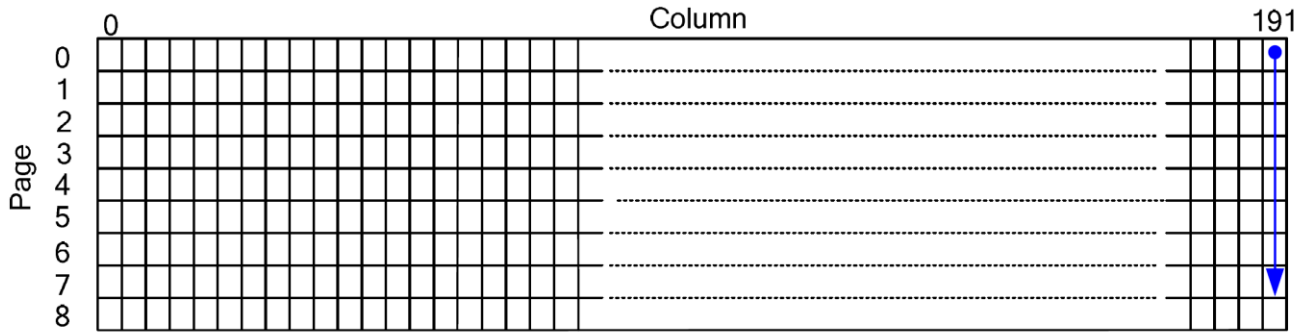


Fig 22. DDRAM Access Mapping (MX=1, AC[2:0]=2, PA[3:0]=0, CA[3:0]=0)

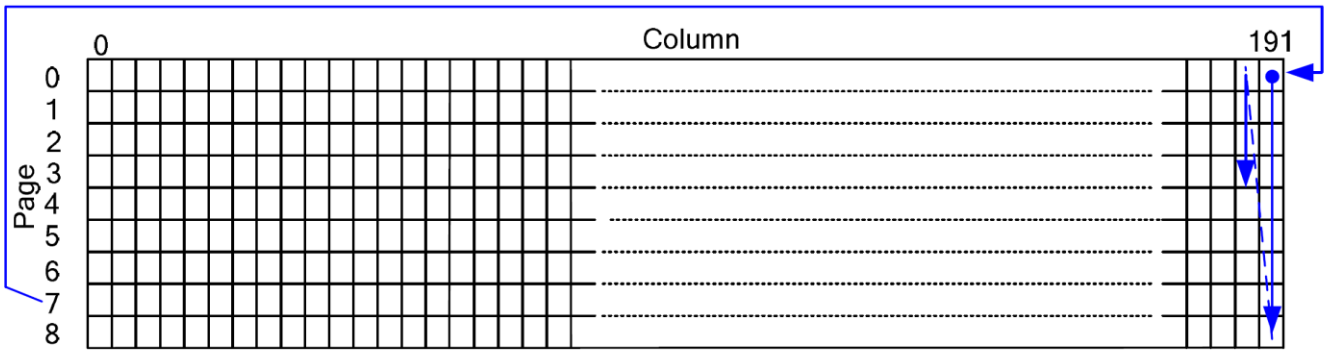


Fig 23. DDRAM Access Mapping (MX=1, AC[2:0]=3, PA[3:0]=0, CA[3:0]=0)

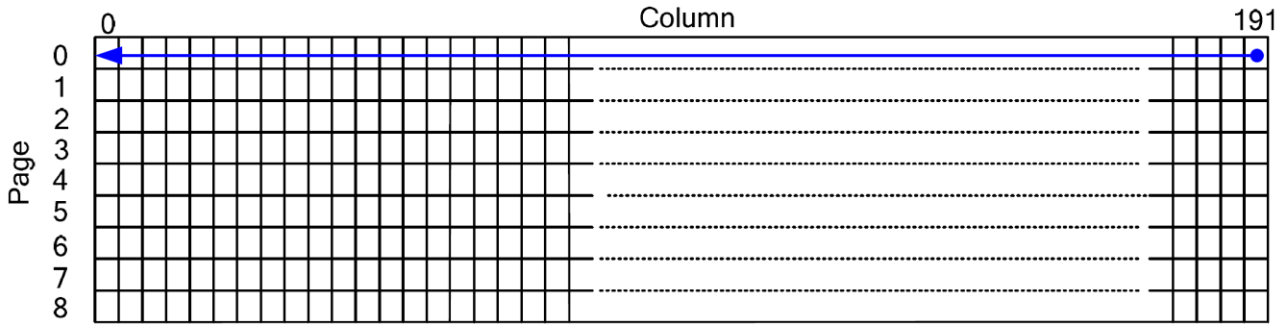


Fig 24. DDRAM Access Mapping (MX=1, AC[2:0]=4, PA[3:0]=0, CA[3:0]=0)

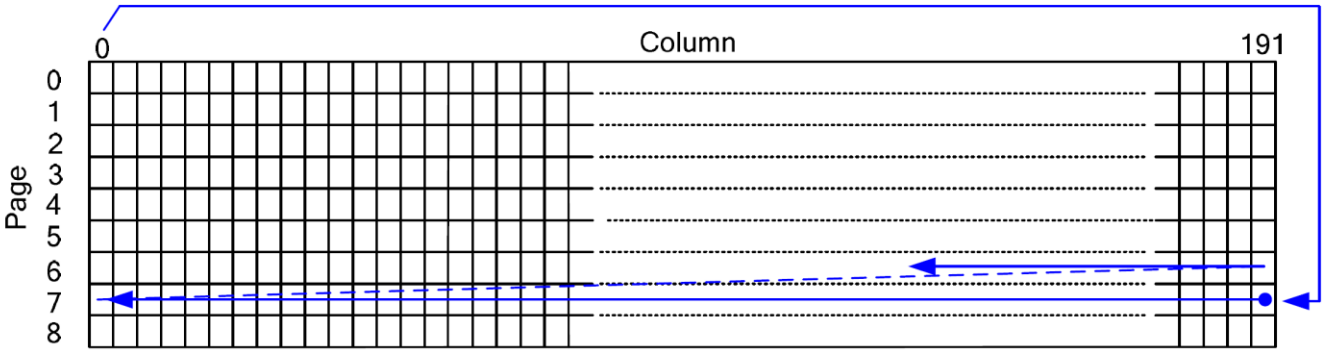


Fig 25. DDRAM Access Mapping (MX=1, AC[2:0]=5, PA[3:0]=7, CA[3:0]=0)

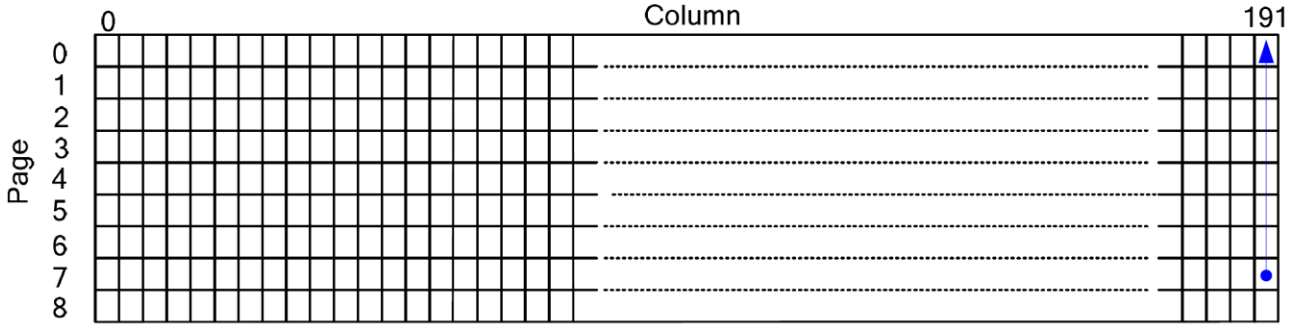


Fig 26. DDRAM Access Mapping (MX=1, AC[2:0]=6, PA[3:0]=7, CA[3:0]=0)

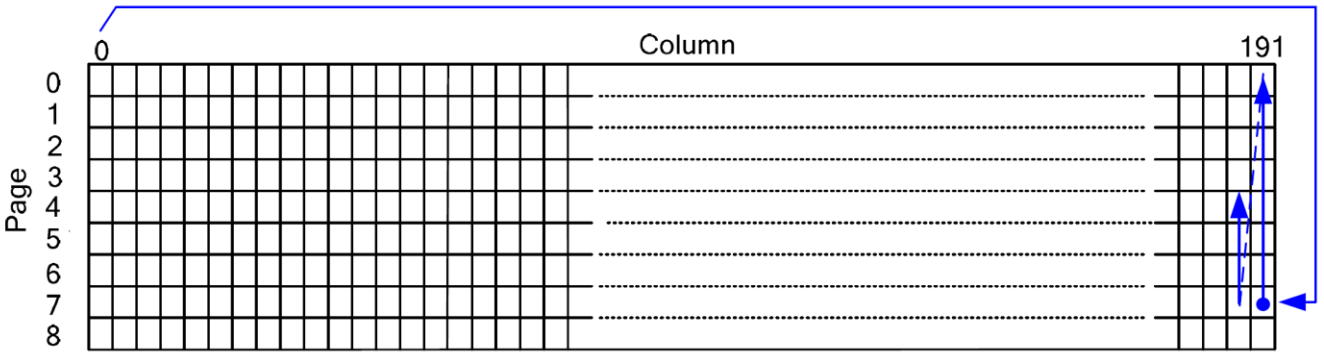
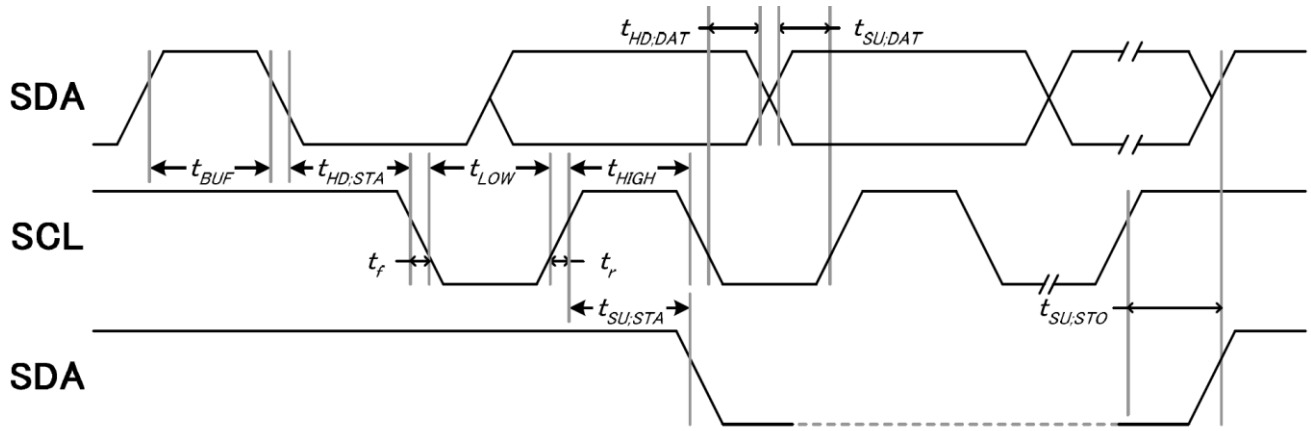


Fig 27. DDRAM Access Mapping (MX=1, AC[2:0]=7, PA[3:0]=7, CA[3:0]=0)

SERIAL INTERFACE TIMING DIAGRAM

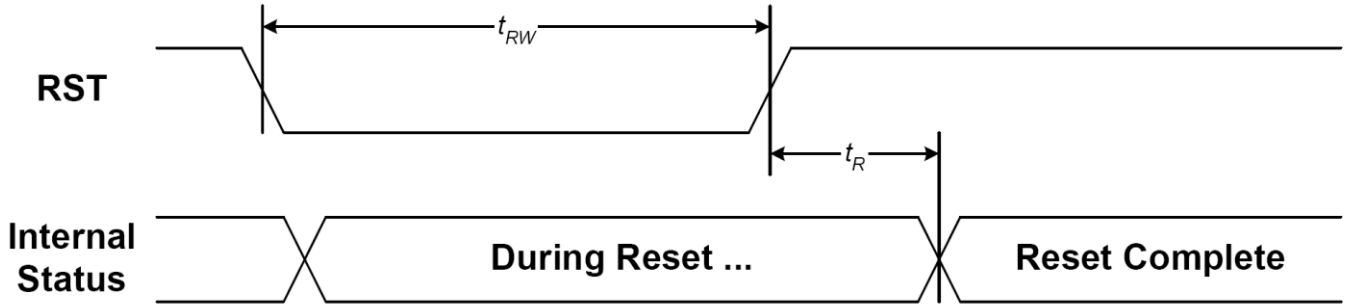


SERIAL INTERFACE TIMING CHARACTERISTICS

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock frequency	SCL	fSCL		-	400	KHz
SCL clock LOW period		tLOW		1.3	-	us
SCL clock HIGH period		tHIGH		0.6	-	
BUS free time between a STOP and START		tBUF		1.3	-	
Data setup time	SDA	tSU;Data		0.1	-	
Data hold time		tHD;Data		0	0.9	
Setup time for a repeated START condition		tSU;STA		0.6	-	
Start condition hold time		tHD;STA		0.6	-	
Setup time for STOP condition		tSU;STO		0.6	-	
Signal rise time	SDA SCL	tr		20+0.1Cb	300	ns
Signal fall time		tf		20+0.1Cb	300	
Capacitive load represented by each bus line		Cb		-	400	pF
Tolerable spike width on bus		tSW		-	50	ns

Note : All timing is specified using 20% and 80% of VDD1 as the standard.

RESET TIMING DIAGRAM



RESET TIMING

(VDD1 = 1.8V ~ 3.3V , Ta =25°C)

Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	1	ms
Reset "L" pulse width	tRW		1	-	

I²C BIT TRANSFER

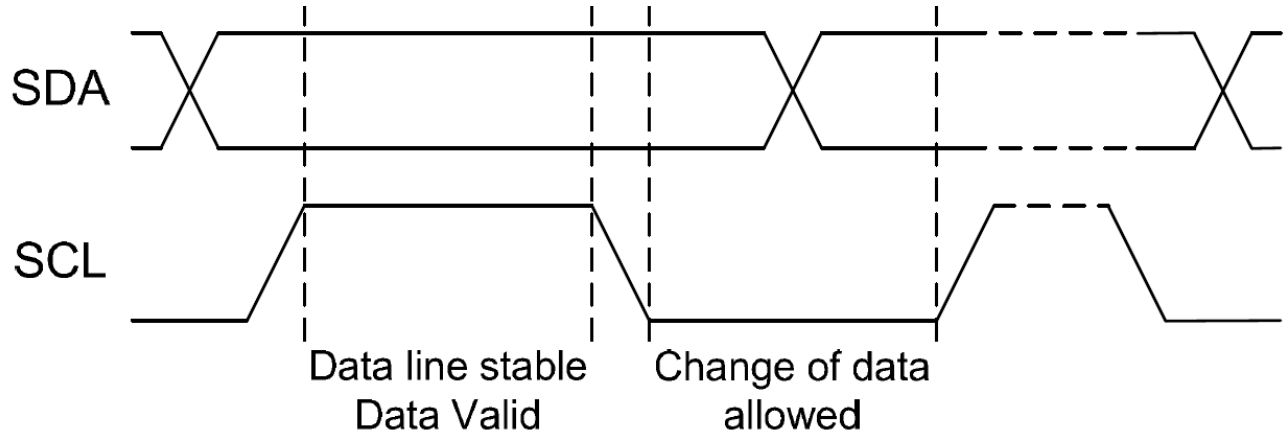


Fig 5. Bit Transfer

START AND STOP CONDITIONS

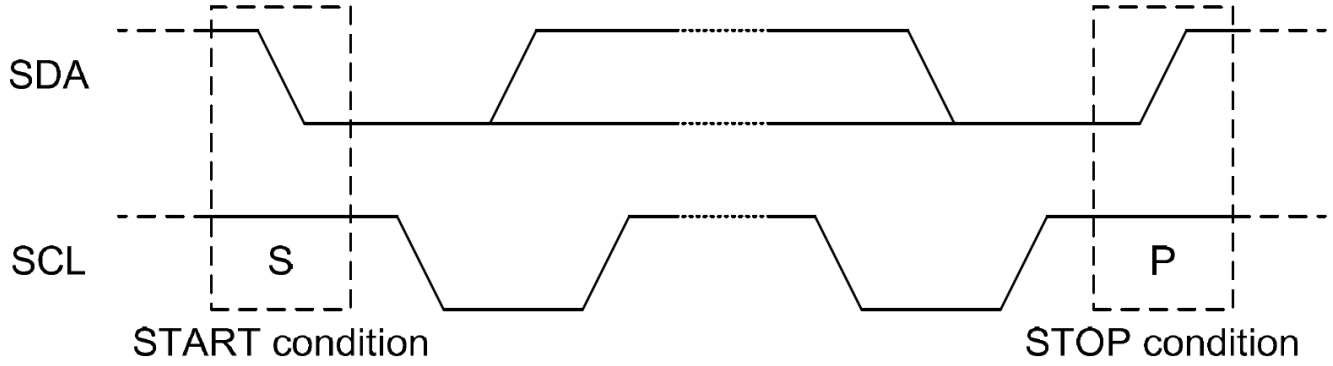


Fig 6. Definition of STRAT and STOP Condition

ACKNOWLEDGEMENT OF I2C INTERFACE

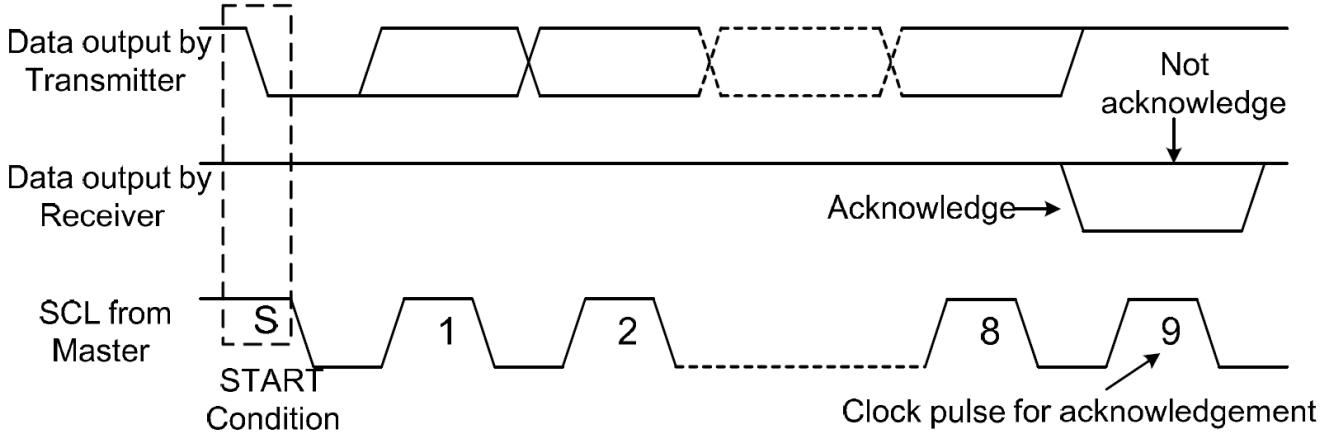


Fig 8. Acknowledgement of I²C Interface

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = VOP / 64 Hz
TEMPERATURE = 22 ± 5 °C
RELATIVE HUMIDITY = 60 ± 15 %

ITEM	SYMBOL	UNIT	TYP. STN
RESPONSE TIME	Ton	ms	150
	Toff	ms	190
CONTRAST RATIO	Cr	-	15
VIEWING ANGLE (6 O'clock) Cr ≥ 2	V3:00	°	45
	V6:00	°	70
	V9:00	°	45
	V12:00	°	60

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

NO.	Item	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
1	High temperature operating	70°C	90°C	240 hours
2	Low temperature operating	-20°C	-40°C	240 hours
3	High temperature storage	80°C	100°C	240 hours
4	Low temperature storage	-30°C	-50°C	240 hours
5	Temperature-humidity storage	60°C 90% R.H.	80°C 90% R.H.	96 hours
6	Temperature cycling	-30°C to 80°C 30 Min Dwell	-50°C to 100°C 30 Min Dwell	5 cycle
7	Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

Inspection condition:
No. 1 ~ 6:
The samples should be placed in room temperature for 2 hours before inspection.

Acceptance criteria:
No non-conformance found in functional and cosmetic.

SAMPLING METHOD
SAMPLING PLAN: ANSI/ASQ Z1.4

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

QUALITY STANDARD

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 4 W DOT MATRIX: IF 0.6 ≤ W, MAX(a,b) < 0.3 N.A.* IF 0.4 ≤ W < 0.6, MAX(a,b) < 0.25 N.A* IF W < 0.4, MAX(a,b) < 0.2 N.A*	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 4 T	MINOR	1
BUBBLES	d* ≥ 0.2 QTY=0	MINOR	2
SPOTS	d ≤ 0.3 N.A.** 0.3<d≤0.4 QTY≤1 0.4<d QTY=0	MINOR	2
LINE SCRATCHES	x≥0.7 y≥0.05 QTY=0	MINOR	3
BLACK LINE	x≥0.7 y≥0.05 QTY=0	MINOR	3

*d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : B

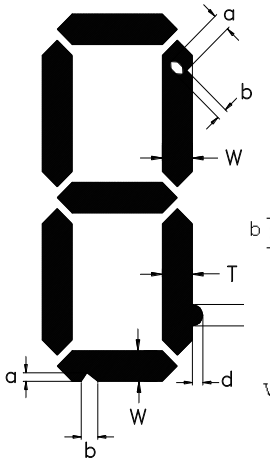
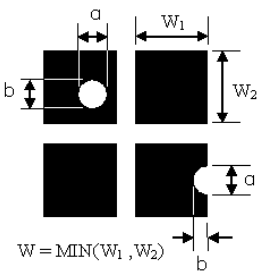
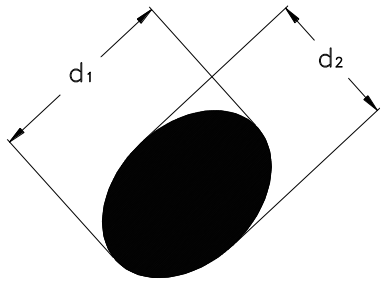
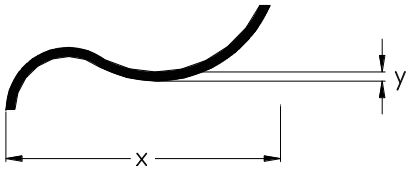


fig . 1





POLARIZER BUBBLES / SPOTS
fig . 2



LINE SCRATCHES / BLACK LINE
fig . 3

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤1/2T f≤1/3W g≤3.5	MINOR	4
	BOTTOM GLASS	p≤1.0 q≤3.5 r≤1/2T		4
	CORNER	a≤1.5 b≤W		4
	TOP GLASS	a≤3.0 b≤1/3T c≤1/2W		5
GLASS PROTRUSION		a ≤ 1/4 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : B

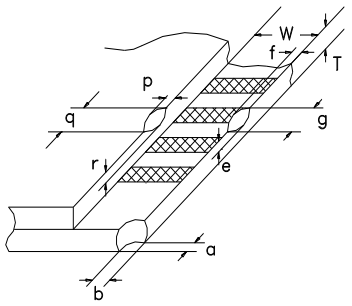


fig . 4

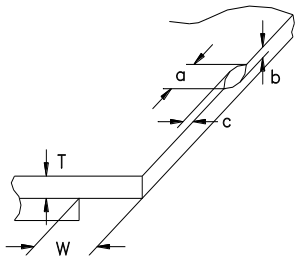


fig . 5

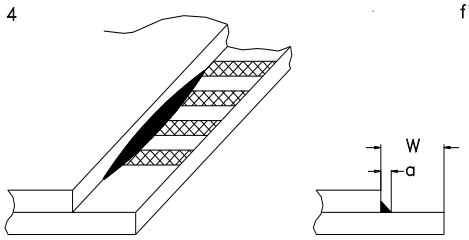


fig . 6

HANDLING PRECAUTIONS (For COG Only)

(1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly.
- Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent;
-water, ketone, aromatics

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to V_{DD} or V_{SS}, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

Remove the protective film slowly and, if possible, under ESD control device like ion blower and humidity of working room should be kept over 50%RH to reduce risk of static charge.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

(4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

(5) SOLDERING (for Pin type)

It is recommended to complete dip soldering at 270 ºC or hand soldering at 280 ºC within 3 seconds. The soldering position is at least 3mm apart from the pin head. Wave or reflow soldering are not recommended. Metal pins should not be soldered for more than 3 times and each soldering should be done after cool down of metal pins

(6) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

WARRANTY

CLOVER will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover is limited to repair and/or replacement. Clover will not be responsible for any subsequent or consequential event.

SPECIFICATION REVISION RECORD

Revision No.	Description	Date(DD/MM/YY)
00	1st Issue	05/07/21