CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model : CG9161B - _ _ - _ _ - _ _ - _

Revision	00
Engineering	KEMP HUANG
Date	3 April 2014
Our Reference	V9055

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MODE OF DISPLAY

Display mode	**Display condition**	**Viewing direction**
☐ TN positive	☐ Reflective type	☐ 6 O' clock
☐ TN negative	☐ Transflective type	☐ 12 O' clock
STN : ☐ Yellow green	☐ Transmissive type	☐ 3 O' clock
☐ Grey	☐ Others	☐ 9 O' clock
☐ Blue (negative)		
☐ FSTN positive		
☐ FSTN negative		

LCD MODULE NUMBER NOTATION:

CG9161B- M Y - E T - N 6 – T
(1) (2) (3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
E – EBTN
*(5)---Rear polarizer type
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)
T – Touch panel (Analog)
P – Touch panel (Digital)

GENERAL DESCRIPTION

Display mode : 16 characters x 1 line COG LCD module

Interface : I^2C or 3-line serial

Driving method : 1/8 duty, 1/4 bias

Controller IC : Sitronix ST7025 or equivalent
For the detailed information, please refer to the IC specifications

MECHANICAL DIMENSIONS

Item	Dimension	Unit
Outline Dimension	113.0(L)x24.4(W)x6.8MAX.(H)	mm
Viewing Area	99.0(L)x14.0(W)	mm
Character Size	4.84(L)x8.06(W)	mm
Character Pitch	6.0(L)x8.56(W)	mm
Dot Size	0.92(L)x1.1(W)	mm

CONNECTOR PIN ASSIGNMENT

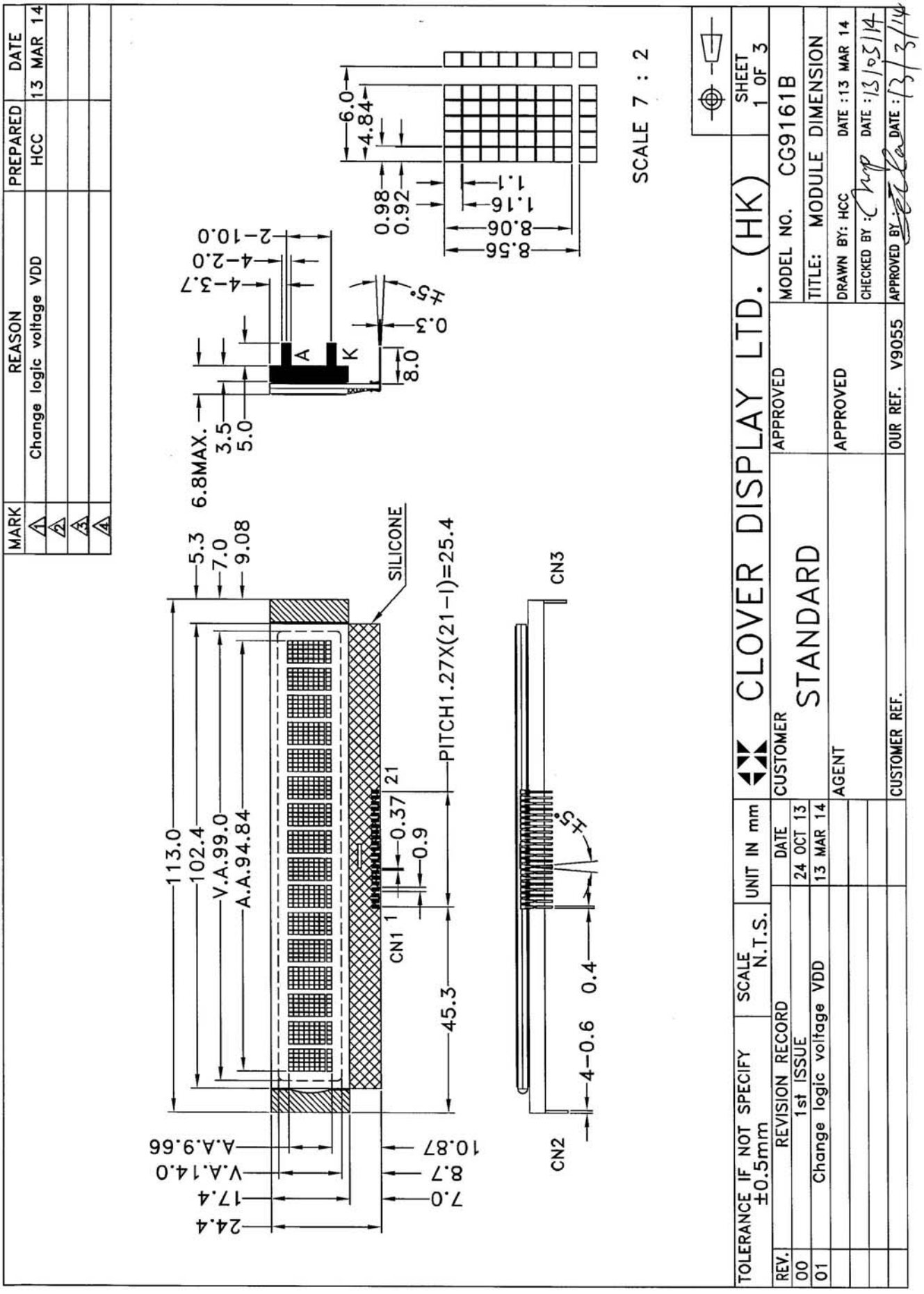
CN1

Pin No.	Signal	Function	Pin No.	Signal	Function
1	VLCD	Supply voltage for LCD	12	VDD	Supply voltage for logic
2	CAP2N	DC/DC voltage converter	13	VD	LCD bias voltage
3	CAP2P		14	SDAP	Serial input data
4	CAP1P		15	SCLP	Serial input clock
5	CAP1N		16	XCSP	Chip select
6	CAP3P		17	XRSTP	Reset
7	V0	LCD bias voltage	18	I2CMS1P	Select I^2C interface address
8	V3		19	IFP	Select MPU interface type
9	V2		20	TYPMDP	Select driving waveform
10	V1		21	LEDPWM	LED backlight control
11	VSS	Ground			

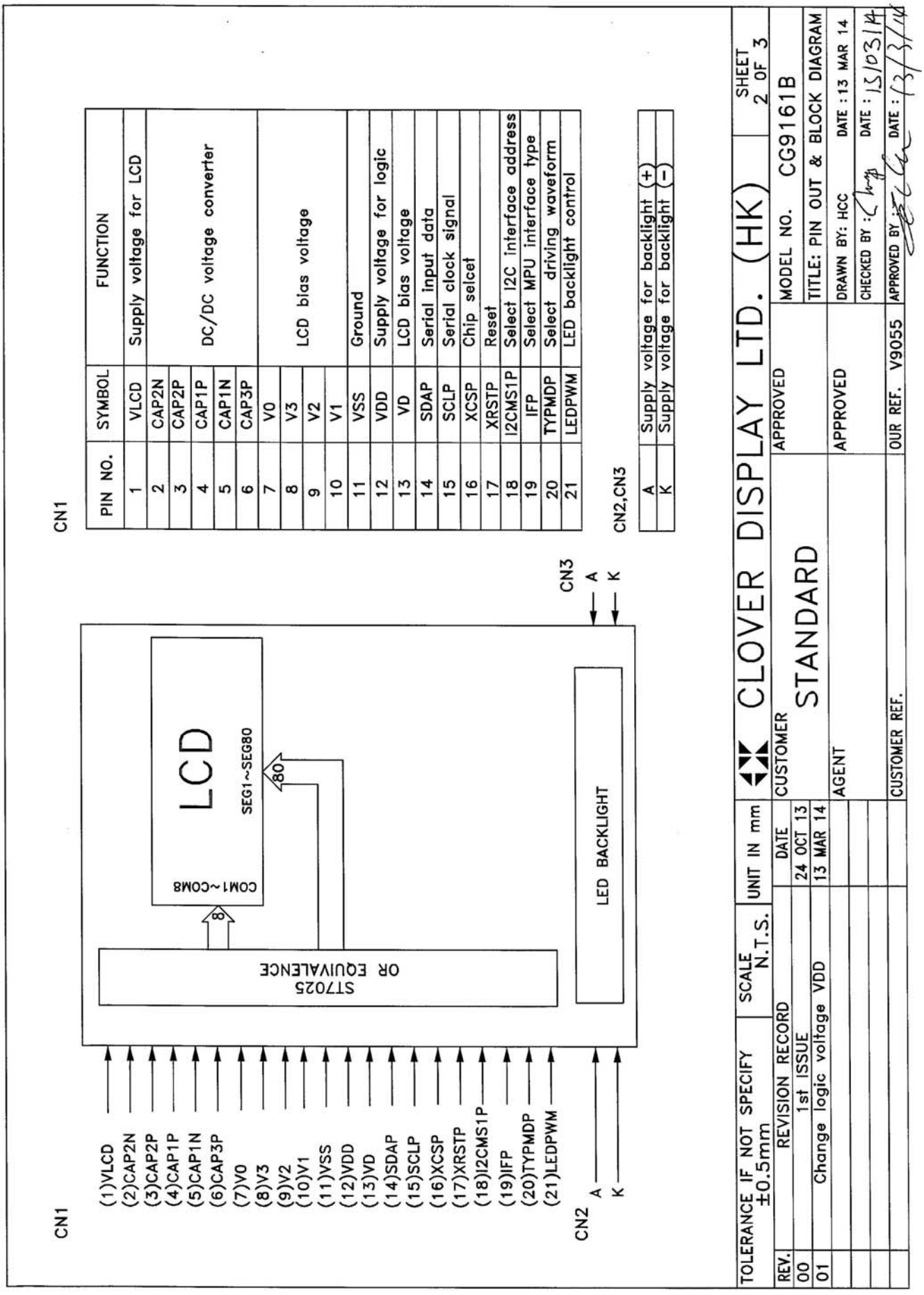
CN2, CN3

	A	Supply voltage for backlight(+)
	K	Supply voltage for backlight(-)

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, @Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	VDD	4.75	5.0	5.25	V
Supply Current	IDD	—	0.84	1.26	mA
Input Voltage for LCD (*)	V0	7.12	7.5	7.88	V
"H" Level Input Voltage	VIH	0.8VDD	—	VDD	V
"L" Level Input Voltage	VIL	VSS	—	0.2VDD	V

Note (*): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Side-lited LED

Constant voltage driving:

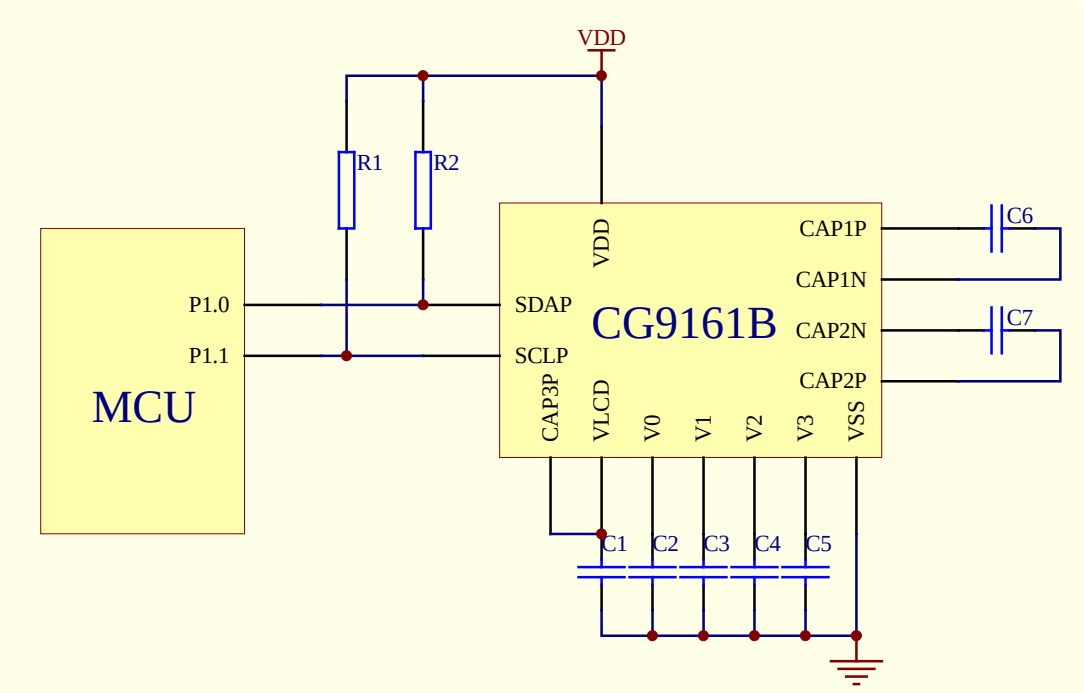
Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
White Backlight current	I_{BL}	-	35	40	mA	V_{BL} = 5.0V

ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage	VDD	-0.3 to 6	-0.3 to 6	V
Input Voltage	VI	-0.3 to VDD +0.3	-0.3 to VDD +0.3	V
Operating Temperature	Topr	0 to 50	-20 to 70	℃
Storage Temperature	Tstg	-10 to 60	-30 to 80	℃

REFERENCE CIRCUIT EXAMPLE



Remark: C1, C2=4.7uF/25V; C3, C4, C5=1uF/16V; C6, C7=1uF/25V.

INSTRUCTIONS

Command	Instruction Code										Description
	Hex	A0	D7	D6	D5	D4	D3	D2	D1	D0	
NOP	00	0	0	0	0	0	0	0	0	0	No Operation
SRESET	01	0	0	0	0	0	0	0	0	1	Software reset
Sleep In	10	0	0	0	0	1	0	0	0	0	Enter Sleep-in mode
Sleep Out	11	0	0	0	0	1	0	0	0	1	Exit Sleep-in mode
Inverse Display OFF	20	0	0	0	1	0	0	0	0	0	Display Inversion off
Inverse Display	21	0	0	0	1	0	0	0	0	1	Display Inversion on
Exit All-Pixel ON	22	0	0	0	1	0	0	0	1	0	All-pixel OFF
All-Pixel ON	23	0	0	0	1	0	0	0	1	1	All-pixel ON
Display OFF	28	0	0	0	1	0	1	0	0	0	Display OFF
Display ON	29	0	0	0	1	0	1	0	0	1	Display ON
Set Column Address	2A	0	0	0	1	0	1	0	1	0	Set column address
	-	1	-	-	-	-	CS3	CS2	CS1	CS0	Column start address
	-	1	-	-	-	-	CE3	CE2	CE1	CE0	Column end address
Set Row Address	2B	0	0	0	1	0	1	0	1	1	Set row address
	-	1	-	-	-	-	RS3	RS2	RS1	RS0	Row start address
	-	1	-	-	-	-	RE3	RE2	RE1	RE0	Row end address
Display Data Length	0F	0	0	0	0	0	1	1	1	1	Set display data length before writing DDRAM (3-Line SPI only)
	-	1	DL7	DL6	DL5	DL4	DL3	DL2	DL1	DL0	
Memory Write	2C	0	0	0	1	0	1	1	0	0	Write data into DDRAM
Power Discharge	D0	0	1	1	0	1	0	0	0	0	Power discharge
	-	1	0	0	0	0	0	0	AD1	AD0	
Set Frame Frequency	B2	0	1	0	1	1	0	0	1	0	Set LCD frame frequency
	-	1	0	0	0	1	FR3	FR2	FR1	FR0	
Set LED PWM	B3	0	1	0	1	1	0	0	1	1	Set PWM waveform for LED backlight
	-	1	-	-	-	-	-	0	LP1	LP0	
	-	1	LEDRT[7:0]								
RAM Counter Direction	B7	0	1	0	1	1	0	1	1	1	Set RAM Counter Direction MX, MY
	-	1	-	-	-	-	-	-	MY	MX	
Set Vop	C0	0	1	1	0	0	0	0	0	0	Set Vop for contrast control. Range: 4V~18V
	-	1	Vop7	Vop6	Vop5	Vop4	Vop3	Vop2	Vop1	Vop0	
	-	1	0	0	0	0	0	0	0	Vop8	
Set Bias	C3	0	1	1	0	0	0	0	1	1	Select Bias for multi-duty
	-	1	0	0	0	0	0	0	BS1	BS0	
Power Control	D2	0	1	1	0	1	0	0	1	0	Power Control
	-	1	0	0	0	OSC	BST	FOL	V0	0	
Set Booster Clock	BA	0	1	0	1	1	1	0	1	0	Set booster clock
	-	1	-	-	-	-	-	BE2	BE1	BE0	

RECOMMENDED INITIAL SETTINGS

Set Reset：01H
Set Column Address：2AH
Set Column Start Address：00H
Set Column End Address：0BH
Set Row Address：2BH
Set Row Start Address：00H
Set Row End Address：08H
Set Display Data Length：0FH,00H
Set VLCD：C0H,78H,00H
Set Memory Write：2CH
Set Bias：C3H,02H
Set Power Control：D2H,1EH
Set RAM Counter Direction：B7H,00H
Display On: 29H

FUNCTION DESCRIPTION

The microprocessor interface of ST7025 can be selected by IF pin to communicate with different type of MPU. Please refer to the table below:

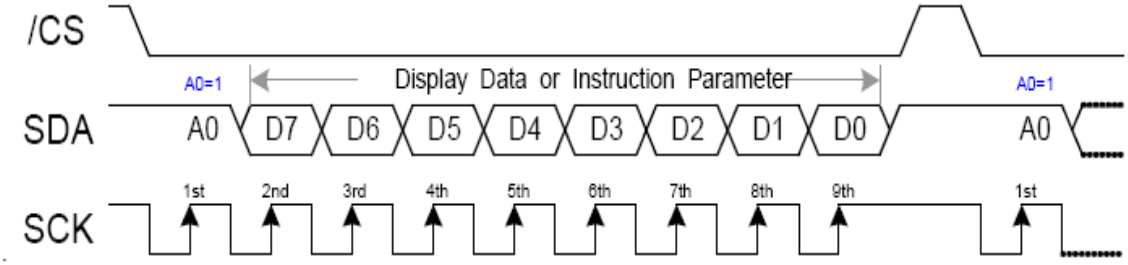
IF Setting	Interface Mode	Available Pins for MPU
H	3-Line SPI (Serial Peripheral Interface)	SDA, SCK, /CS, /RST
L	I^2C compatible interface	SDA, SCK, /RST

3-Line SPI Interface (9-bit)

The 3-Line SPI (9-bit) uses 3 pins (/CS, SDA & SCK) to communicate with MPU. When /CS is "L", IC is active and the SDA and SCK pins are enabled. Serial data is latched at the rising edge of serial clock. The internal shift register collects serial bits and reformat them into 8-bit data after the last (9^{th}) clock. After /CS returns to "H", IC is inactive and the internal shift register and counter are reset. The parameter/command indicator is the "A0" bit: the 1^{st} bit of each 9-bit serial data.

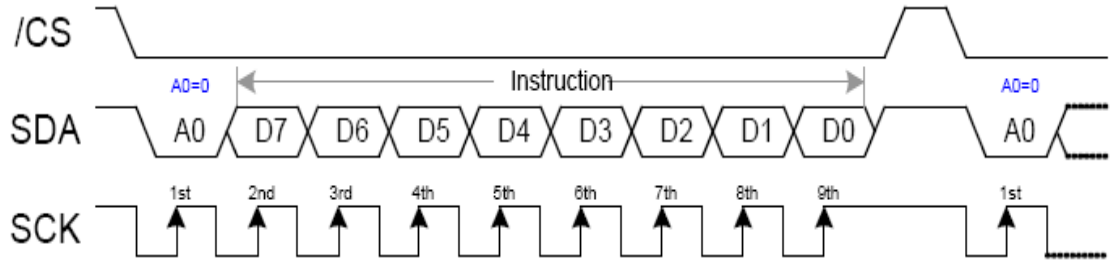
Write Parameter by 3-Line SPI (A0=1)

When A0 is "1", the transferred 8-bit is parameter.



Write Instruction by 3-Line SPI (A0=0)

When A0 is "0", the transferred 8-bit is instruction.



FUNCTION DESCRIPTION(CONT.)

I²C Compatible Interface

The I²C Compatible Interface is for bi-directional, two-line communication between different ICs or modules. The two lines are a Serial Data line (SDA) and a Serial Clock line (SCL). Both lines must be connected with a pull-up resistor which drives SDA and SCL to high when the bus is not busy. Data transfer can be initiated only when the bus is not busy.

BIT TRANSFER

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse because changes of SDA line at this time will be interpreted as START or STOP. Bit transfer is illustrated in Fig. 4.

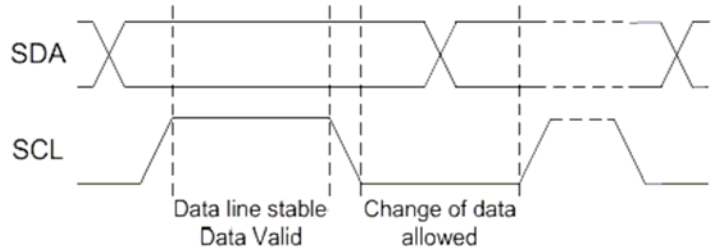


Fig. 4 Bit Transfer

START AND STOP CONDITIONS

Both SDA and SCL lines remain HIGH when the bus is not busy. A HIGH-to-LOW transition of SDA while SCL is HIGH, is defined as the START condition (S). A LOW-to-HIGH transition of SDA while SCL is HIGH, is defined as the STOP condition (P). The START and STOP conditions are illustrated in Fig. 5.

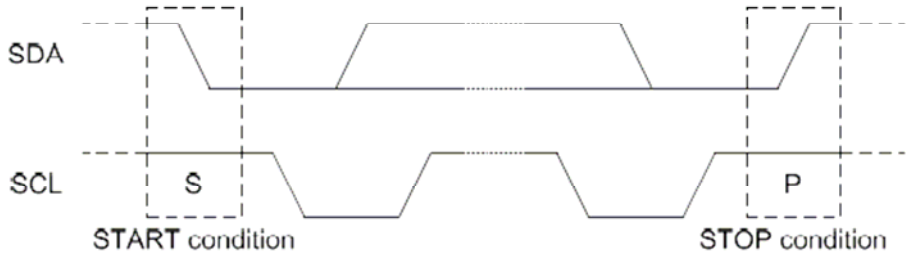
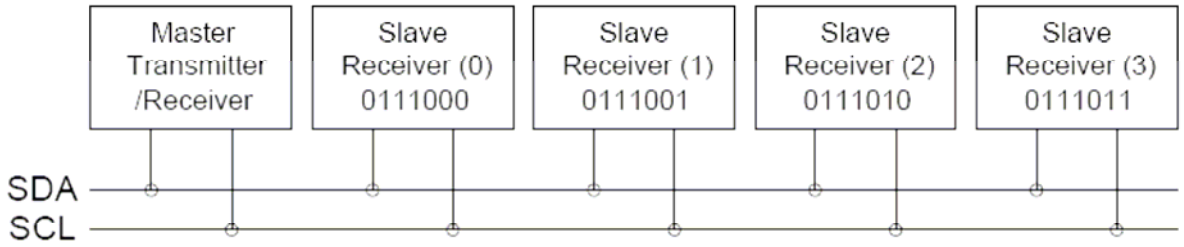


Fig. 5 Definition of START and STOP Condition

SYSTEM CONFIGURATION

The system configuration is illustrated in Fig. 6. Word-definitions are explained below:

- Transmitter: the device which sends the data to the bus.
- Receiver: the device which receives the data from the bus.
- Master: the device which initiates a transfer, generates clock signals and terminates a transfer.
- Slave: the device which is addressed by a master.



FUNCTION DESCRIPTION(CONT.)

I²C INTERFACE PROTOCOL

ST7025 supports command/data write to addressed slaves on the bus.

Before any data is transmitted on the I²C Interface, the device which should respond is addressed first. For 7-bit slave addresses (0111**00**, 0111**01**, 0111**10** and 0111**11**) are reserved for ST7025. The least significant 2 bits of the slave address is set by connecting I2CMS0 and I2CMS1 to either logic 0 (VSS1) or logic 1 (VDD1).

The I²C Interface protocol is illustrated in Fig. 8.

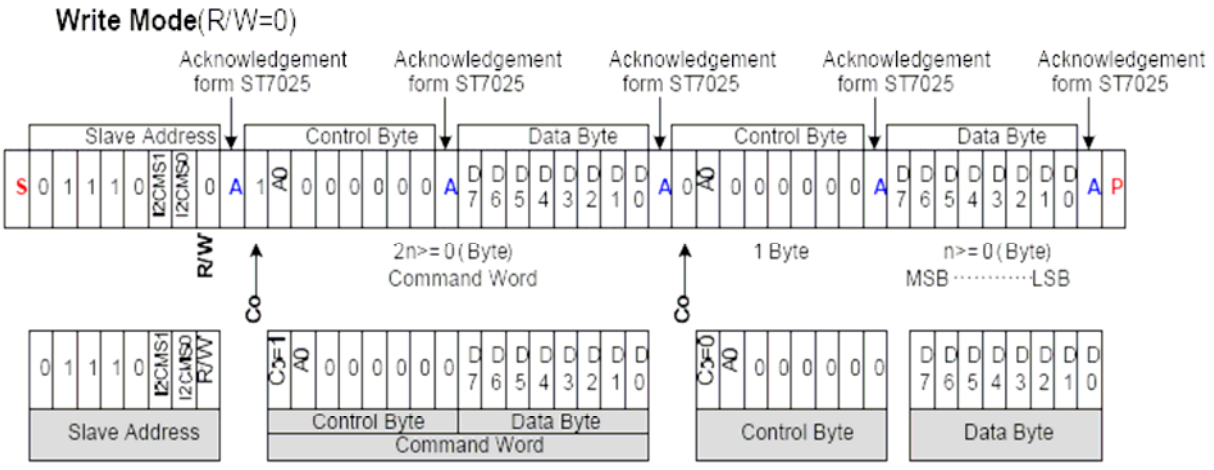
The sequence is initiated with a START condition (S) from the I²C Interface master, which is followed by the slave address. All slaves with the corresponding address acknowledge in parallel, all the others will ignore the I²C Interface transfer. After acknowledgement, one or more command are followed and the status of the addressed slaves is defined. A command word consists of a control byte, which defines Co and A0, and a data byte.

The last control byte is tagged with a cleared bit (i.e. the continuation bit Co). After a control byte with a cleared Co bit, only data byte(s) will follow. The state of the A0 bit defines whether the following data bytes are interpreted as commands or as RAM data. All addressed slaves on the bus also acknowledge the control and data bytes. After the last control byte, either a series of display data bytes or command data bytes may follow (depending on the A0 bit setting).

If the A0 bit of the last control byte is set to logic 1, these data bytes (display data bytes) will be stored in the display RAM at the address specified by the internal data pointer. The data pointer is automatically updated and the data is directed to the intended ST7025 device.

If the A0 bit of the last control byte is set to logic 0, these data bytes (command data byte) will be decoded and the setting of ST7025 will be changed according to the received commands.

Only the addressed slave makes the acknowledgement after each byte. At the end of the transmission the bus master issues a STOP condition (P). If no acknowledge is generated by the master after a byte, the driver stops transferring data to the master.



Co	0	Last control byte. Only a stream of data bytes is allowed to follow. This stream may only be terminated by a STOP or RE-START condition.
	1	Another control byte will follow the data byte.

DISPLAY DATA RAM (DDRAM)

Data Format & DDRAM Structure

The display data is written through D0 to D7.

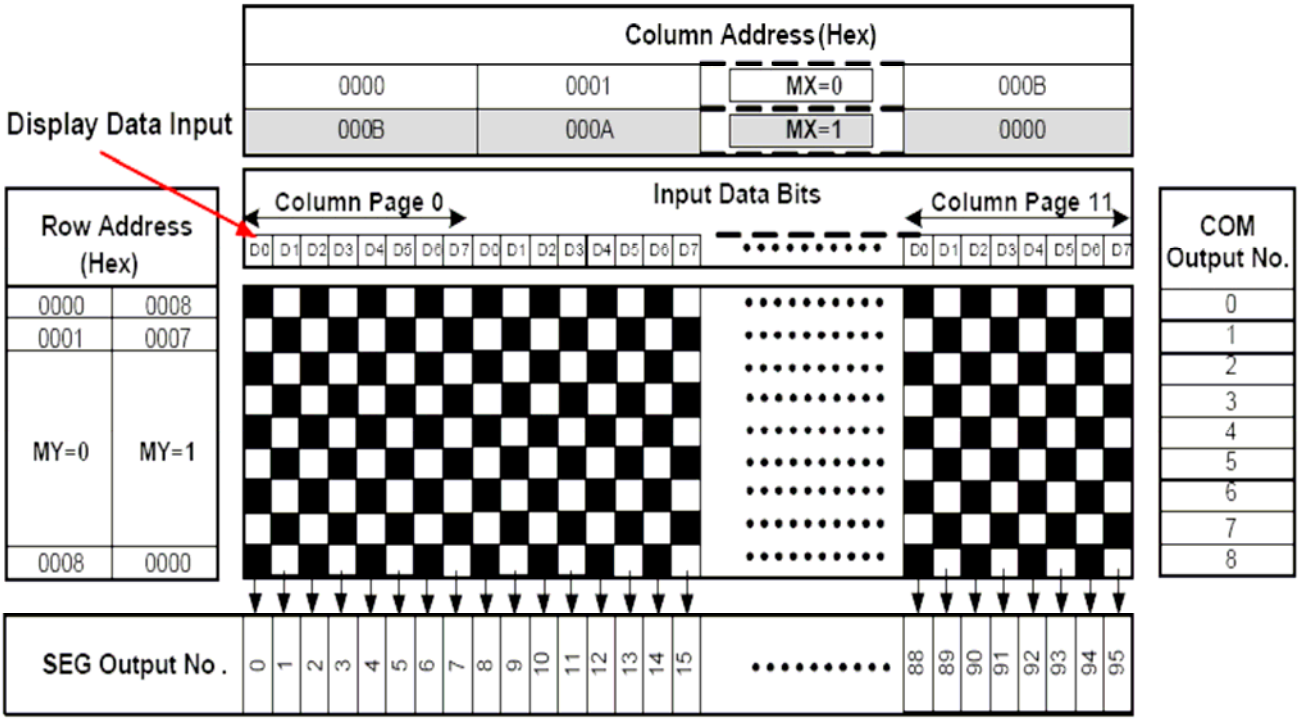
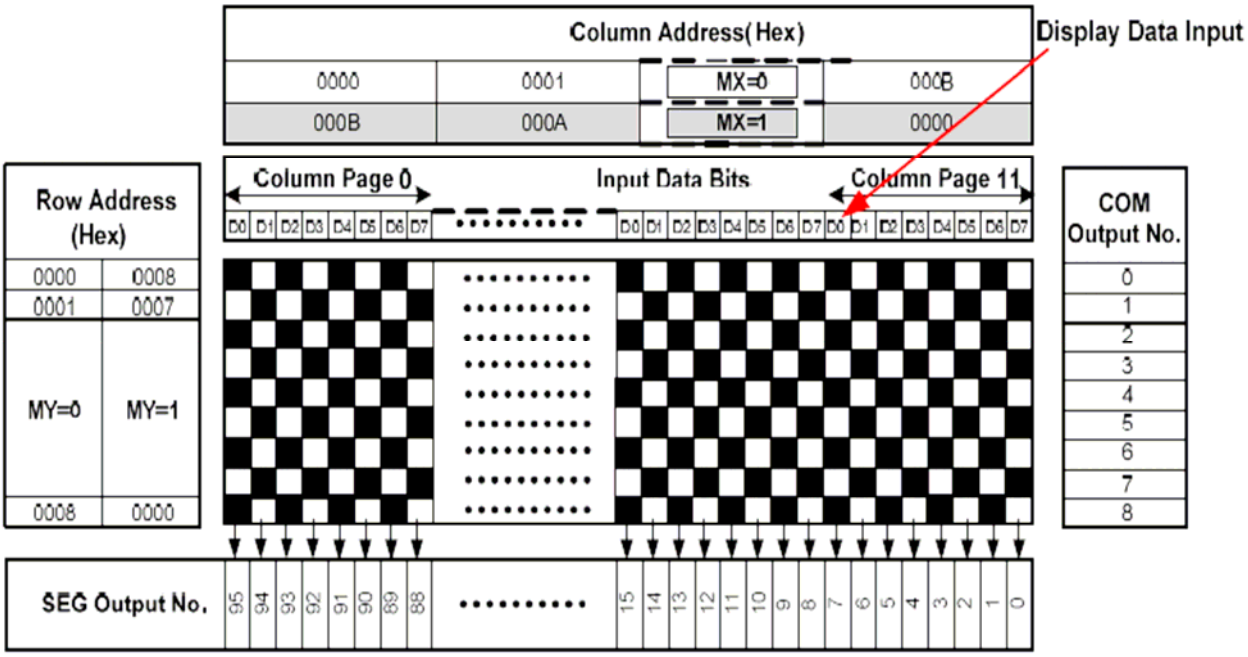


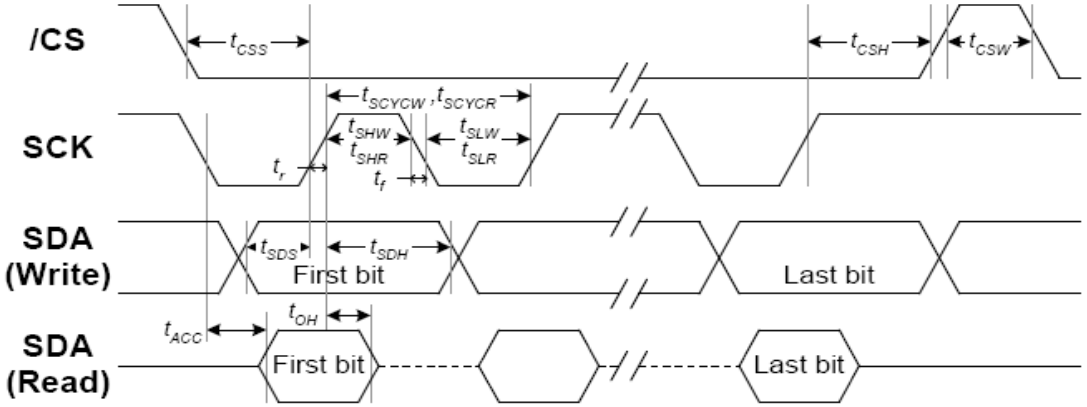
Fig. 12 Data Format and DDRAM Structure

Sometimes, a mirrored DDRAM map is easier for manual data mapping.



AC CHARACTERISTICS

SPI 3-LINE SERIAL INTERFACE TIMING



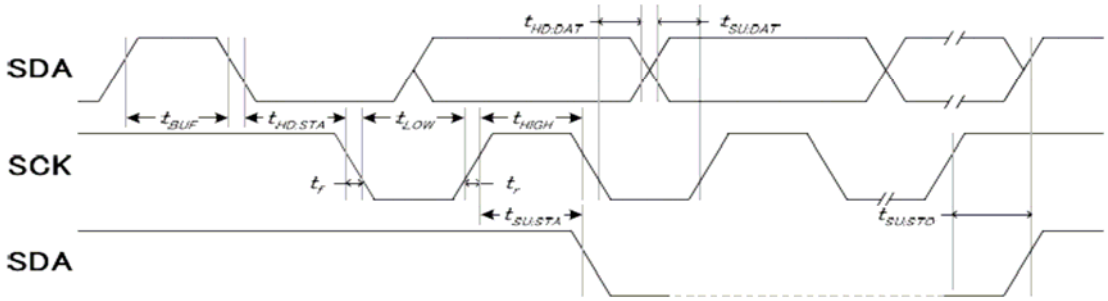
(VDD1=3~5V Ta=25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock period (Write)	SCK	tSCYCW		250	—	ns
SCK "H" pulse width		tSHW		100	—	
SCK "L" pulse width		tSLW		100	—	
Data setup time	SDA	tSDS		100	—	
Data hold time		tSDH		100	—	
Chip select setup time	/CS	tCSS		150	—	
Chip select hold time		tCSH		150	—	
Chip select wait time		tCSW		20	—	

*1 The rise and fall time (tr, tf) of the input signal are specified at 15 ns or less.

*2 All timings take 20% and 80% of VDD as standard.

I²C INTERFACE TIMING

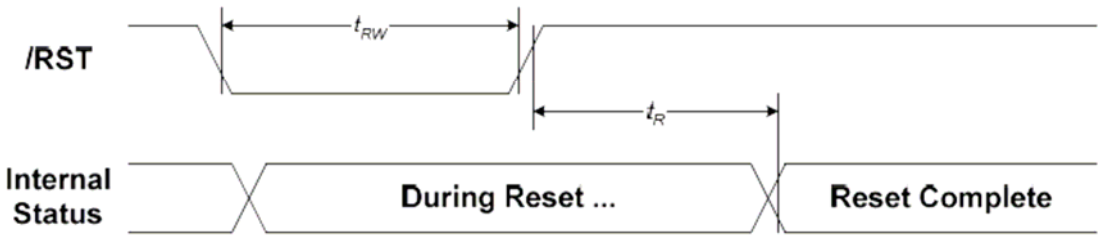


(VDD=3~5V, Ta=25℃)

Item	Signal	Symbol	Condition	Min.	Max.	Unit
Serial clock frequency	SCK	fSCL		-	400	KHz
SCL clock LOW period		tLOW		1.3	-	us
SCL clock HIGH period		tHIGH		0.6	-	
BUS free time between a STOP and START		tBUF		1.3	—	
Data setup time	SDA	tSU;Data		0.1	—	
Data hold time		tHD;Data		0.02	—	
Setup time for a repeated START condition		tSU;STA		0.6	—	
Start condition hold time		tHD;STA		0.6	—	
Setup time for STOP condition		tSU;STO		0.6	—	
Signal rise time (Min: C_L=40pF; Max: C_L=400pF)	SDA SCK	tr		—	300	ns
Signal fall time (Min: C_L=40pF; Max: C_L=400pF)		tf		—	300	
Tolerable spike width on bus		tSW		—	15	

*1 All timings take 20% and 80% of VDD as standard.

RESET TIMING



(VDD=3~5V Ta=25℃)

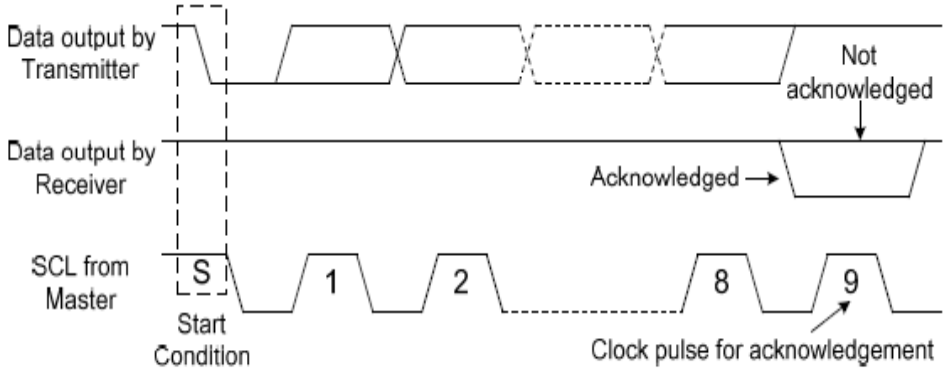
Item	Symbol	Condition	Min.	Max.	Unit
Reset time	tR		-	2	us
Reset "L" pulse width	tRW		2.5	-	

*1 The rise and fall time (tr, tf) input signal are specified at 15 ns or less.

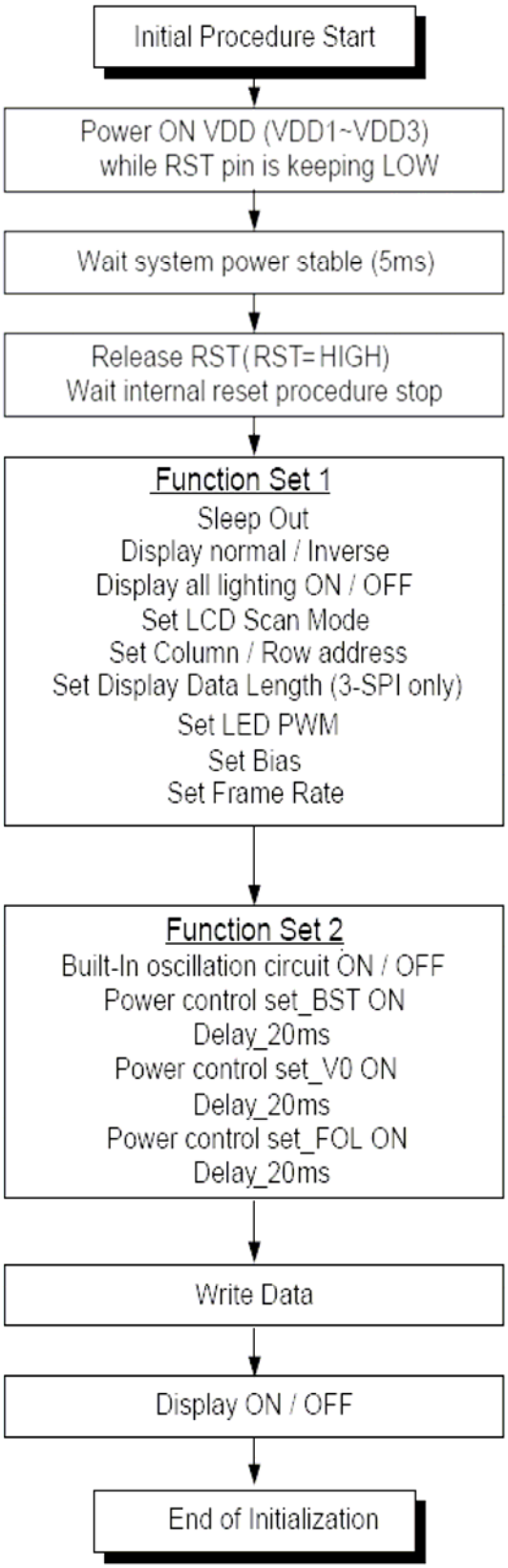
*2 All timings take 20% and 80% of VDD as standard.

ACKNOWLEDGEMENT OF I2C INTERFACE

Each byte of eight bits is followed by an acknowledge-bit. The acknowledge-bit is a HIGH signal put on SDA by the transmitter when the master generates an extra acknowledge-related clock pulse. A slave receiver addressed must generate an acknowledge-bit after the reception of each byte. The device that acknowledges must pull-down the SDA line during the acknowledge-clock pulse, so that the SDA line stays LOW during the HIGH period of the acknowledge-related clock pulse (set-up and hold times must be taken into consideration). Acknowledgement on the I^2C Interface is illustrated in Fig. 7.



INITIAL FLOW (WITH BUILT-IN POWER CIRCUITS)



Power ON and Initial Flow Notes:

1. To prevent power ON noise, please hold RST LOW until the system power is stable (generally 5ms)
2. After releasing RST signal (RST=High), do NOT issue instruction immediately. An internal reset time (tR) is required for finishing internal reset procedure.
3. The delay time for Power Control flow depends on LCD module. The delay time should be increased if the ITO resistance or capacitor value increases.
4. The build-in DDRAM content is unknown after power ON. The content cannot be reset by hardware or software reset. It is recommended to add a DDRAM initial flow to prevent unexpected display pattern after turning ON the display.

THE RESET CIRCUIT

Setting /RST to "L" (hardware reset) can initialize internal function. /RST pin must connect to the reset pin of MPU and initialization by /RST pin is essential before operating. When /RST becomes "L" or "SRESET" instruction is issued, the internal reset procedure will start. The procedure is listed below:

Internal oscillator: OFF
Internal LCD PWM circuits: OFF
Display: OFF (all SEGs/COMs output VSS level)
Display all-point: Exit
Inverse Display: OFF
Row address: 0
Column address: 0
Power control [OSC, BST, FOL, V0] = All OFF
All registers are default value

After power-on, display data in DDRAM is undefined and the display status is "Display OFF". The contents in DDRAM will not be cleared by internal reset procedure. It's better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON. Besides, the power is not stable when it is just turned ON. A hardware reset is needed to initialize those internal registers after the power is stable.

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = VOP / 64 Hz
TEMPERATURE = 23 ± 5 °C
RELATIVE HUMIDITY = 60 ± 20 %

ITEM	SYMBOL	UNIT	TYP.
RESPONSE TIME	Ton	ms	60
	Toff	ms	80
CONTRAST RATIO	Cr	-	500
VIEWING ANGLE (Cr ≥ 2)	V3:00	°	85
	V6:00	°	85
	V9:00	°	85
	V12:00	°	50

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

NO.	Item	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
1	High temperature operating	50°C	70°C	240 hours
2	Low temperature operating	0°C	-20°C	240 hours
3	High temperature storage	60°C	80°C	240 hours
4	Low temperature storage	-10°C	-30°C	240 hours
5	Temperature-humidity storage	40°C 90% R.H.	60°C 90% R.H.	96 hours
6	Temperature cycling	-10°C to 60°C 30 Min Dwell	-30°C to 80°C 30 Min Dwell	5 cycle
7	Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

Inspection condition:
No. 1 ~ 6:
The samples should be placed in room temperature for 2 hours before inspection.

Acceptance criteria:
No non-conformance found in functional and cosmetic.

SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

QUALITY STANDARD

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 3 W	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 3 T	MINOR	1
BUBBLES	d* ≥ 0.7 QTY=0	MINOR	2
SPOTS	d ≤ 0.7 N.A.** 0.7<d≤0.8 QTY≤2 0.8<d QTY=0	MINOR	2
LINE SCRATCHES	x≥0.7 y≥0.05 QTY=0	MINOR	3
BLACK LINE	x≥0.7 y≥0.05 QTY=0	MINOR	3

*d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : F

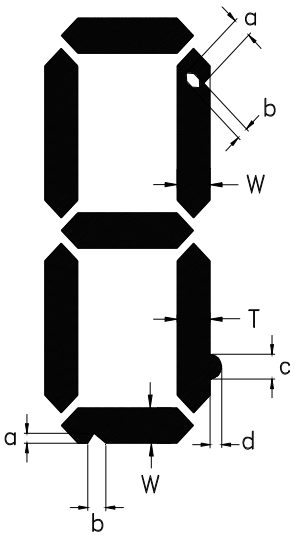
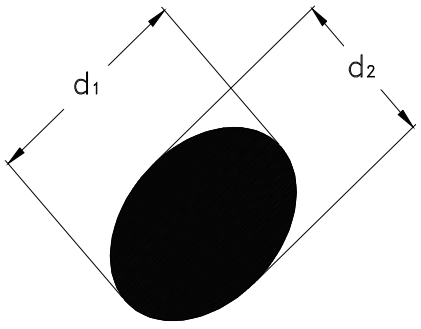
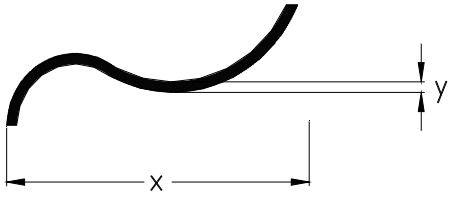


fig . 1



POLARIZER BUBBLES / SPOTS
fig . 2



LINE SCRATCHES / BLACK LINE
fig . 3

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤T f≤1/2W g:N.A.	MINOR	4
	BOTTOM GLASS	p≤V.A.*** q:N.A. r≤T		4
	CORNER	a:N.A. b≤W		4
	TOP GLASS	a:N.A. b≤T c≤W		5
GLASS PROTRUSION		a ≤ 1/3 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE, ALL UNIT ARE IN MILLIMETER. ***CANNOT EXTEND IN V.A. DEFECT TABLE: F

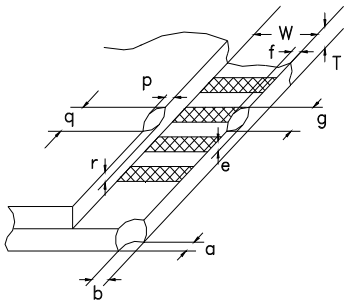


fig . 4

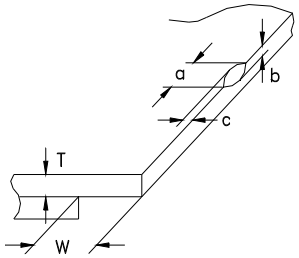


fig . 5

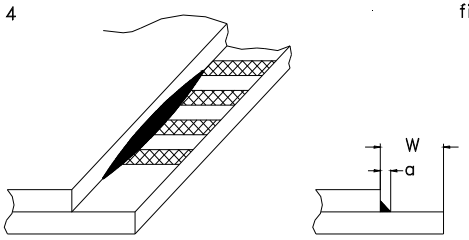


fig . 6

QUALITY STANDARD OF LCD MODULE

1.0	**Sampling Method**		
	Sampling Plan : MIL STD 105 E Class of AQL : Level II/Single Sampling Critical : 0.25% Major 0.65% Minor 1.5%		
2.0	**Defect Group**	**Failure Category**	**Failure Reasons**
	Critical Defect 0.25%(AQL)	Malfunction	Open Short Burnt or dead component Missing part/improper part P.C.B. Broken
	Major Defect 0.65%(AQL)	Poor Insulation	Potential short High current Component damage or scratched or Lying too close improper coating
		Poor Conduction	Damage joint Wrong polarity Wrong spec. part Uneven/intermittent contact Loose part Copper peeling Rust or corrosion or dirt‘s
	Minor Defect 1.5%(AQL)	Cosmetic Defect	Minor scratch Flux residue Thin solder Poor plating Poor marking Crack solder Poor bending Poor packing Wrong size

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly.
- Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent;
-water, ketone, aromatics

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to V_{DD} or V_{SS}, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

Remove the protective film slowly and, if possible, under ESD control device like ion blower and humidity of working room should be kept over 50%RH to reduce risk of static charge.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

(4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

(5) SOLDERING (for Pin type)

It is recommended to complete dip soldering at 270 ^{o}C or hand soldering at 280 ^{o}C within 3 seconds. The soldering position is at least 3mm apart from the pin head. Wave or reflow soldering are not recommended. Metal pins should not be soldered for more than 3 times and each soldering should be done after cool down of metal pins**.**

(6) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

WARRANTY

CLOVER will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover is limited to repair and/or replacement. Clover will not be responsible for any subsequent or consequential event.

APPENDIX

LOT INDICATION OF LCD MODULE

CODING SYSTEM:

1 DIGIT COLOR CODE: 1

↓

Month

COLOR CODE:

MONTH	COLOR	
1	BROWN	棕
2	RED	紅
3	ORANGE	橙
4	YELLOW	黃
5	GREEN	綠
6	BLUE	藍
7	PURPLE	紫
8	GREY	灰
9	WHITE	白
10	BLACK	黑
11	GOLD	金
12	SILVER	銀

3 TYPES OF LOCATION AS SHOWN BELOW: