CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model: CG240128A - _ _ - _ _ - _ _ - _

Revision	03
Engineering	KY LAM
Date	07 March 2025
Our Reference	X9035

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MODE OF DISPLAY

Display mode	**Display condition**	**Viewing direction**
STN : ☐ Yellow green	☐ Reflective type	☐ 6 O' clock
☐ Grey	☐ Transflective type	☐ 12 O' clock
☐ Blue (negative)	☐ Transmissive type	☐ 3 O' clock
☐ FSTN positive	☐ Others	☐ 9 O' clock
☐ FSTN negative		

LCD MODULE NUMBER NOTATION:

CG240128A- N N - S R - N 6 – T
(1) (2) (3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
T – TN
V – TN (Negative)
S – STN Yellow green
G – STN Grey
B – STN Blue (Negative)
F – FSTN
N – FSTN (Negative)
*(5)---Rear polarizer type
R – Reflective
F – Transflective
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)

GENERAL DESCRIPTION

Display mode : 240 X 128 dots, graphic COG LCD module

Interface : 4/8 bit parallel(8080/6800) / 3 line or 4 line SPI

Driving method : 1/128 duty, 1/12 bias

Controller IC : Ultra Chip UC1608 or equivalent
For the detailed information, please refer to the IC specifications.
In the event of any discrepancies between this specification and IC specification, the IC specification shall prevail.

MECHANICAL DIMENSIONS

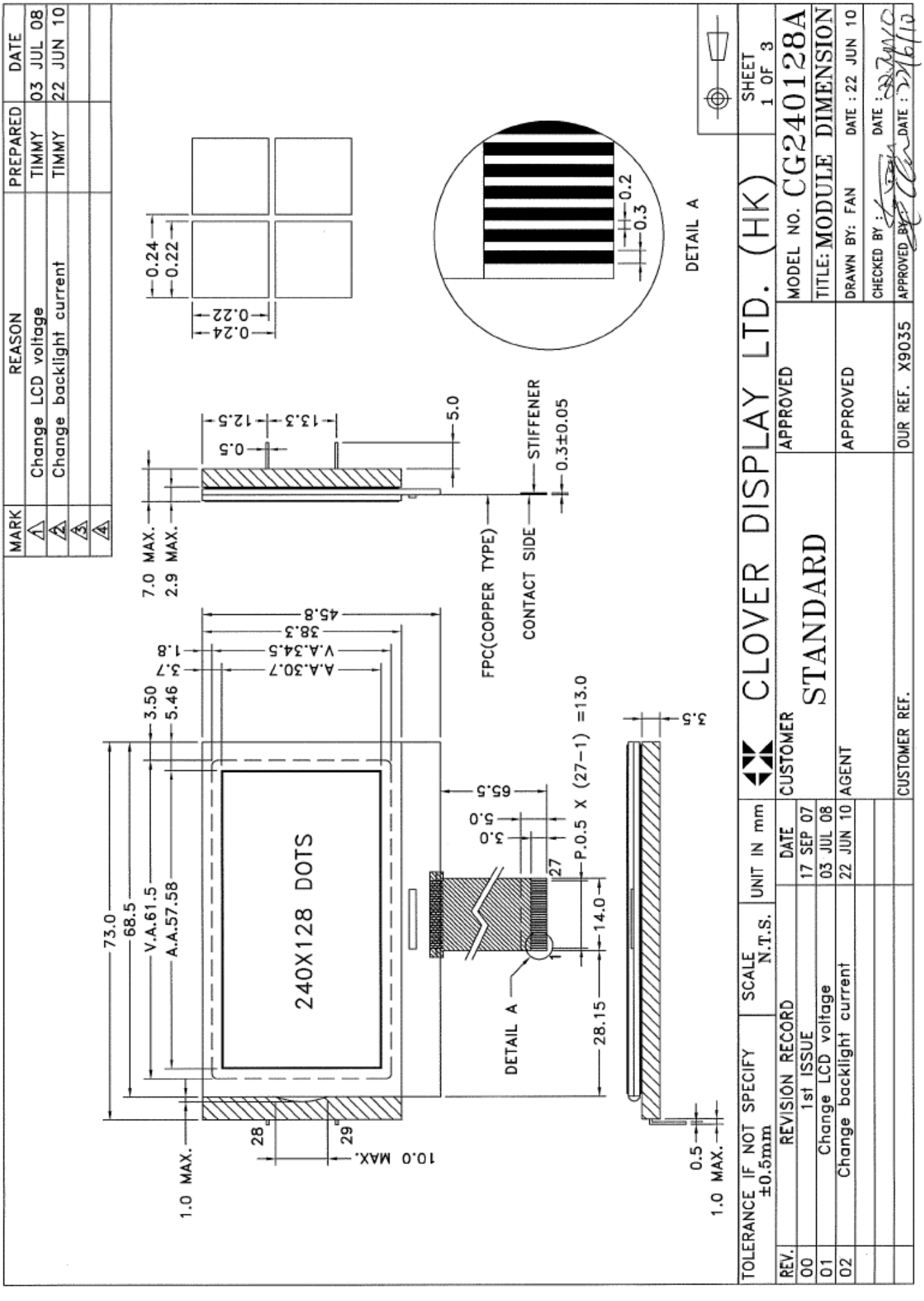
Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension			Viewing Area	61.5 (L)x34.5(W)	mm
Non Backlight (N)	68.5(L) x 45.8(W) x 2.9MAX(H)	mm	Dot Pitch	0.24(L)x0.24(W)	mm
LED Sided Backlight(L)	73.0(L) x 45.8(W) x 7.0MAX(H)	mm	Dot Size	0.22(L)x0.22(W)	mm

CONNECTOR PIN ASSIGNMENT

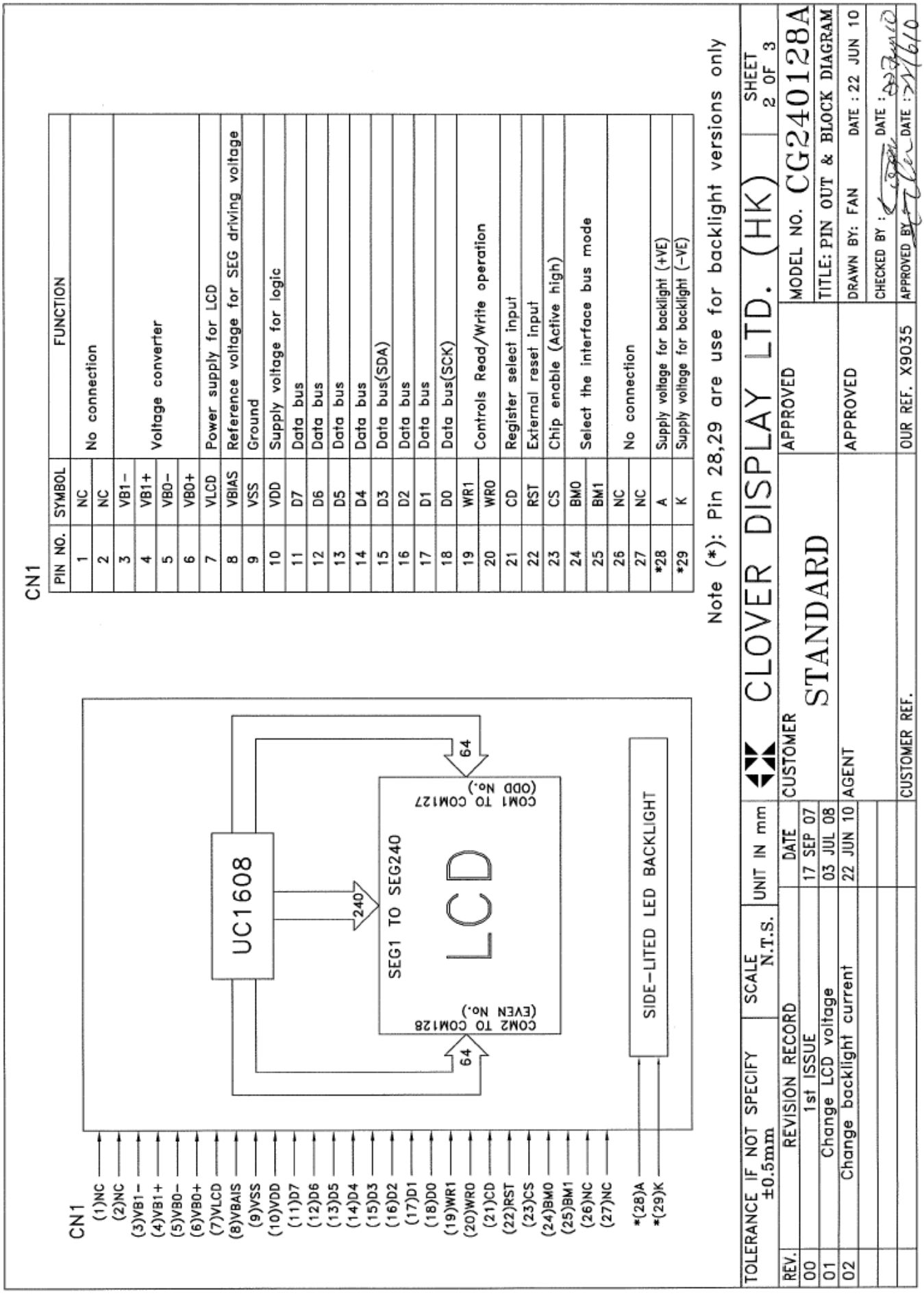
Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	No connection	16	D2	Data bus
2	NC		17	D1	
3	VB1-	Voltage converter	18	D0	Data bus(SCK)
4	VB1+		19	WR1	Controls Read/Write operation
5	VB0-		20	WR0	
6	VB0+		21	CD	Register select input
7	VLCD	Power supply for LCD	22	RST	External reset Input
8	VBIAS	Reference voltage for SEG driving voltage	23	CS	Chip enable (Active High)
9	VSS	Ground	24	BM0	Select the interface bus mode
10	VDD	Supply voltage for logic	25	BM1	
11	D7	Data bus	26	NC	No connection
12	D6		27	NC	
13	D5		*28	A	Supply voltage for backlight (+VE)
14	D4		*29	K	Supply voltage for backlight (-VE)
15	D3	Data bus(SDA)			

Note (*) : Pin 28,29 are used for backlight version

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit	Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage for Logic	VDD	3.05	3.30	3.55	V	"H"Level Input Voltage	VIH	0.8VDD	–	–	V
Supply Current for Logic	IDD	–	0.76	1.14	mA	"L"Level Input Voltage	VIL	–	–	0.2VDD	V
Power supply for LCD control (*)	VLCD	13.3	14.0	14.7	V	–	–	–	–	–	–

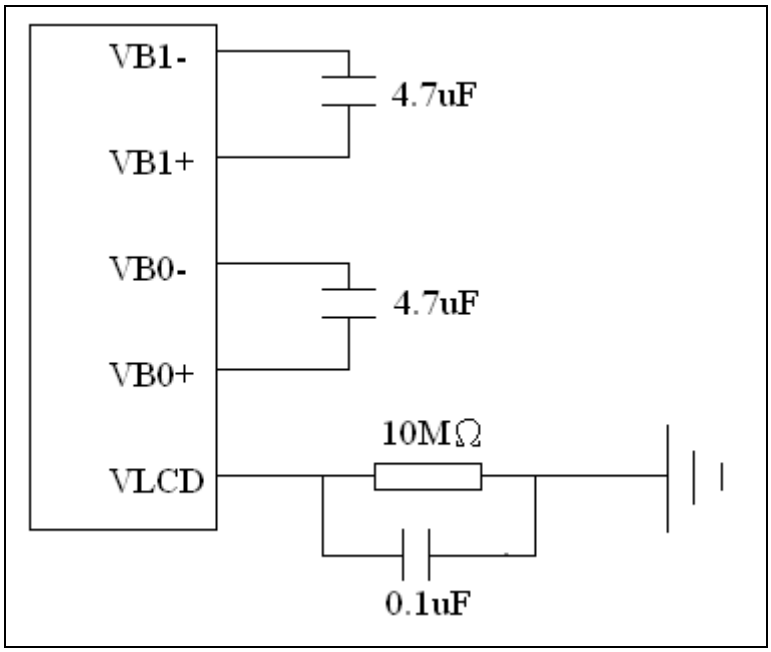
Note (*): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Side Backlight:

Constant voltage driving:

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Backlight current	IBL	-	30	35	mA	VBL = 5.0V

REFERENCE CIRCUIT EXAMPLE



ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage	V_{DD}	-0.3 to 4.0	-0.3 to 4.0	V
Input Voltage	V_T	-0.4 to V_{DD} +0.5	-0.4 to V_{DD} +0.5	V
Operating Temperature	T_{opr}	0 to 50	-20 to 70	℃
Storage Temperature	T_{stg}	-10 to 60	-30 to 80	℃

COMMANDS TABLE

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1	Get Status	N/A
4	Set Column Address LSB	0	0	0	0	0	0	#	#	#	#	Set CA[3:0]	0
	Set Column Address MSB	0	0	0	0	0	1	#	#	#	#	Set CA[7:4]	0
5	Set Mux Rate and temperature compensation.	0	0	0	0	1	0	0	#	#	#	Set {MR, TC[1:0]}	MR: 1b TC: 00b
6	Set Power Control	0	0	0	0	1	0	1	#	#	#	Set PC[2:0]	101b
7	Set Adv. Program Control. (double byte command)	0	0	0	0	1	1	0	0	0	R	For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		
8	Set Start Line	0	0	0	1	#	#	#	#	#	#	Set SL[5:0]	0
9	Set Gain and Potentiometer (double-byte command)	0	0	1	0	0	0	0	0	0	1	Set {GN[1:0], PM[5:0]}	GN=3 PM=0
		0	0	#	#	#	#	#	#	#	#		
10	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
11	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0=disable
12	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0=disable
13	Set Display Enable	0	0	1	0	1	0	1	1	1	#	Set DC[2]	0=disable
14	Set Fixed Lines	0	0	1	0	0	1	#	#	#	#	Set FL[3:0]	0
15	Set Page Address	0	0	1	0	1	1	#	#	#	#	Set PA[3:0]	0
16	Set LCD Mapping Control	0	0	1	1	0	0	#	#	#	#	Set LC[3:0]	0
17	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
18	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
19	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	10b=12
20	Reset Cursor Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	N/A
21	Set Cursor Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	N/A
22	Set Test Control (double byte command)	0	0	1	1	1	0	0	1	TT		For UltraChip only. Do not use.	N/A
		0	0	#	#	#	#	#	#	#	#		

* Other than commands listed above, all other bit patterns may result in undefined behavior.

COMMAND DESCRIPTION

(1) Write data to display memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Write data	1	0	8bits data write to SRAM							

(2) Read data to display memory

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Read data	1	1	8bits data from SRAM							

Write/Read Data Byte (command 1,2) operations access display buffer RAM based on Page Address (PA) register and Column Address (CA) register. To minimize bus interface cycles, PA and CA will be incremented automatically depending on the setting of Access Control (AC) registers. PA and CA can also be programmed directly by issuing *Set Page Address* and *Set Column Address* commands.

If Wrap-Around (WA) is OFF (AC[0] = 0), CA will stop increasing after reaching the end of page (MC), and system programmers need to set the values of PA and CA explicitly. If WA is ON (AC[0]=1), when CA reaches end of page, CA will be reset to 0 and PA will be increased or decrease by 1, depending on the setting of Page Increment Direction (PID, AC[2]). When PA reaches the boundary of RAM (i.e. PA = 0 or 15), PA will be wrapped around to the other end of RAM and continue.

(3) Get Status

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Get Status	0	1	BZ	MX	DE	RS	WA	GN1	GN0	1

Status flag definitions:

BZ: Busy with internal process.
MX: Status of register LC[2], mirror X.
DE: Display enable flag. DE=1 when display enabled
RS: Reset in progress. If RS=1, host interface will be inaccessible.
WA: status of register AC[0]. Automatic column/page wrap around.
GN0, 1: GN[1:0]. register Gain

(4) Set Column Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Column Address LSB CA[3:0]	0	0	**0**	**0**	**0**	**0**	CA3	CA2	CA1	CA0
Set Column Address MSB CA[7:4]	0	0	**0**	**0**	**0**	**1**	CA7	CA6	CA5	CA4

Set the SRAM column address before Write/Read memory from host interface.

CA possible value=**0-239**

(5) Set Multiplex Rate and Temperature Compensation

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Multiplex Rate MR Set Temperature Compensation TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	MR	TC1	TC0

Set the multiplex ratio (number of rows) and temperature compensation.

MUX ratio definition: 0b=96 **1b=128**

Temperature compensation curve definition:

00b= -0.00%/C 01b= -0.05%/C 10b= -0.10%/C 11b= -0.20%/C

(6) Set Power Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Panel Loading PC[2:0]	0	0	**0**	**0**	**1**	**0**	**1**	PC2	PC1	PC0

Set PC[1:0], according to the capacitance loading of LCD panel.

Panel loading definition:

00b: LCD < 26 nF **01b: 26 nF < LCD < 43 nF**

10b: 43 nF < LCD < 60nF 11b: 60nF < LCD < 90 nF

Set PC[2] to program to use internal charge pump of external V_{LCD} source.

Pump control definition:

0b=External V_{LCD} **1b=Internal V_{LCD}**

(7) Set Advanced Program Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set APC[0]	0	0	**0**	**0**	**1**	**1**	**0**	**0**	**0**	R
(Double byte command)	0	0	APC register parameter							

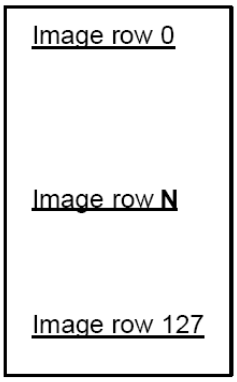
For UltraChip only. Please Do NOT use.

(8) Set Start Line

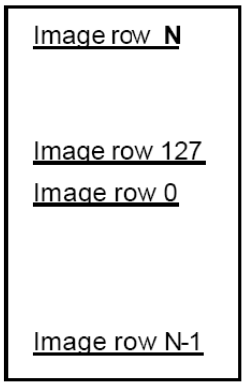
Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Start Line SL[5:0]	0	0	**0**	**1**	SL5	SL4	SL3	SL2	SL1	SL0

Set the start line number

Start line setting will scroll the displayed image up by SL rows. The valid value is between 0 (no scrolling) and 63. One example of the visual effect on LCD is illustrated in the figure below.



SL=0



SL=N

(9) Set Gain and Potentiometer

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Gain and Potentiometer	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
GN [1:0] PM [5:0] (Double byte command)	0	0	GN1	GN0	PM5	PM4	PM3	PM2	PM1	PM0

Program Gain (GN[1:0]) and Potentiometer (PM[5:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range of GN = **0 ~ 3** PM value = **0 ~ 63**

(10) Set RAM Address Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0] - WA, Automatic column/page wrap around.
0: CA or PA (depends on AC[1]= 0 or 1) will stop incrementing after reaching boundary
1: CA or PA (depends on AC[1]= 0 or 1) will restart, and PA or CA will increment by one step.

AC[1] – Reserved (always set to **0**)

AC[2] – PID, page address (PA) auto increment direction (**0**/1 = +/- 1)
When WA=1, controls whether page address will be adjusted by +1 or -1, when CA reached CA boundary.
No effect when WA=0.

CA boundary is 239 and PA boundary is 15 when PID=0, PA boundary is 0 when PID=1.

(11) Set All Pixel ON

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set All Pixel On DC [1]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**0**	DC1

Set DC[1] to force all SEG drivers to output ON signals. This function has no effect on the existing data stored in display RAM.

(12) Set Inverse Display

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Inverse Display DC [0]	0	0	**1**	**0**	**1**	**0**	**0**	**1**	**1**	DC0

Set DC[0] to force all SEG drivers to output the inverse of the data stored in display memory. This function has no effect on the existing data stored in display RAM.

(13) Set Display Enable

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Enable DC[2]	0	0	**1**	**0**	**1**	**0**	**1**	**1**	**1**	DC2

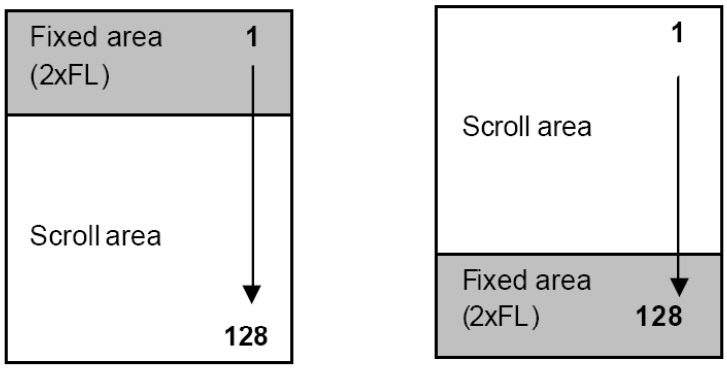
This command is for programming registers DC[2].

When DC[2] is set to 0, the IC will put itself into Sleep mode. All drivers, voltage generation circuit and timing circuit will be halted to conserve power. When DC[2] is set to 1, UC1608 will first exit from Sleep mode, restore the power and then turn on COM drivers and SEG drivers. There is no other explicit user action or timing sequence required to enter or exit the Sleep mode.

(14) Set Fixed Lines

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Fixed Lines FL [3:0]	0	0	1	0	0	1	FL3	FL2	FL1	FL0

The fixed line function is used to implement the partial scroll function by dividing the screen into scroll and fixed area. Set Fixed Lines command will define the fixed area, which will not be affected by the SL scroll function. The fixed area covers the top 2xFL rows for mirror Y (MY) is 0 and bottom 2xFL rows for MY=1. One example of the visual effect on LCD is illustrated in the figure below.



MY = 0 MY = 1

(15) Set Page Address

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page Address LSB PA [3:0]	0	0	1	0	1	1	PA3	PA2	PA1	PA0

Set the SRAM page address before write/read memory from host interface.
Effective range of value = **0 ~ 15**

(16) Set LCD Mapping Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC[3:0]	0	0	1	1	0	0	MY	MX	0	MSF

Set LC[3:0] for COM (row) mirror (MY), SEG (column) mirror (MX) and MSB first or LSB first options (MSF).

MY is implemented by reversing the mapping order between RAM and COM (row) electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

MX is implemented by selecting the CA or 239-CA as write/read (from host interface) display RAM column address so this function will only take effect after rewriting the RAM data.

MSF is implemented by MSB-LSB swapping. When MSB first (LC[0]) bit is set, data D[7:0] will be re-aligned as D[0:7] then be stored to RAM.

(17) System Reset

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	1	1	1	0	0	0	1	0

This command will activate the system reset. The system will take about 15ms to reset

(18) NOP

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
No operation	0	0	1	1	1	0	0	0	1	1

This command is used for “no operation”.

(19) Set LCD Bias Ratio

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	1	1	1	0	1	0	BR1	BR0

Bias ratio definition:

00b= 10.7 01b=11.3 **10b=12.0** 11b=12.7

(20) Reset Cursor Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Return to Cursor. AC[3]=0, CA=CR	0	0	1	1	1	0	1	1	1	0

This command is used to reset cursor update mode function. See description below.

(21) Set Cursor Mode

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC[3]=1 CR=CA	0	0	1	1	1	0	1	1	1	1

Set Cursor Mode command is used to turn on cursor update mode function. AC[3] will be set to 1, register CR will be set to the value of register CA

When AC[3]=1, column address (CA) will only increment with write RAM operation but not on read RAM operation. The address CA wraps around will also be suspended no matter what WA setting is. The purpose of this combination of features is to support " Read-Modify-Write" for cursor implementation.

Reset Cursor Mode command will clear cursor update mode flag (AC[3]=0), CA will be restored to previous CA value which is stored in CR, and CA, PA increment will return to its normal condition.

(22) Set Test Control

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set TT (Double byte command)	0	0	1	1	1	0	0	1	TT	
	0	0	Testing parameter							

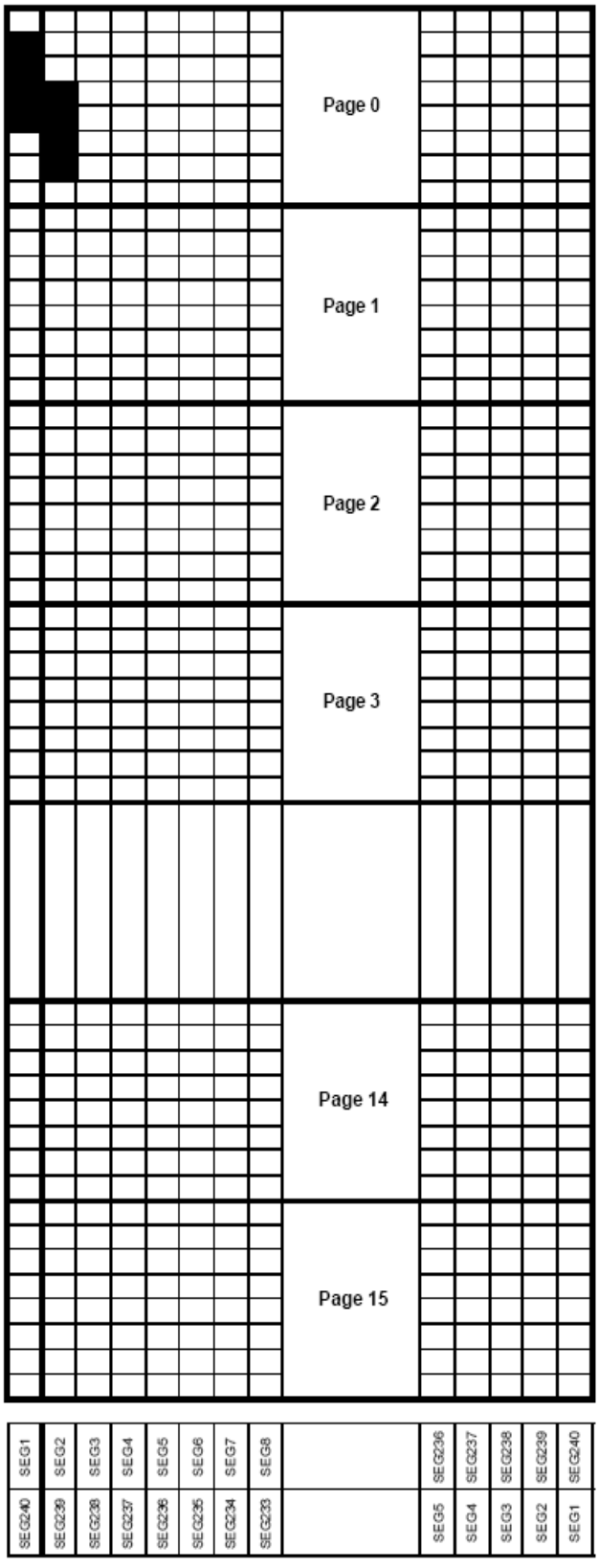
This command is used for UltraChip production testing. For UltraChip Only. Please do not use.

RECOMMENDED INITIAL SETTINGS

Set Power Control：2FH
Set Multiplex Rate And Temperature Compensation：27H
Set LCD Mapping Control：C8H
Set LCD Bias Ratio：E9H
Set Gain Potentiometer：5EH
Set RAM Address Control：89H
Set Start Line：40H
Set Display Enable：AFH

THE ADDRESS CIRCUIT

MSF 0	MSF 1	Line Address
D0	D7	00H
D1	D6	01H
D2	D5	02H
D3	D4	03H
D4	D3	04H
D5	D2	05H
D6	D1	06H
D7	D0	07H
D0	D7	08H
D1	D6	09H
D2	D5	0AH
D3	D4	0BH
D4	D3	0CH
D5	D2	0DH
D6	D1	0EH
D7	D0	0FH
D0	D7	10H
D1	D6	11H
D2	D5	12H
D3	D4	13H
D4	D3	14H
D5	D2	15H
D6	D1	16H
D7	D0	17H
D0	D7	18H
D1	D6	19H
D2	D5	1AH
D3	D4	1BH
D4	D3	1CH
D5	D2	1DH
D6	D1	1EH
D7	D0	1FH
D0	D7	70H
D1	D6	71H
D2	D5	72H
D3	D4	73H
D4	D3	74H
D5	D2	75H
D6	D1	76H
D7	D0	77H
D0	D7	78H
D1	D6	79H
D2	D5	7AH
D3	D4	7BH
D4	D3	7CH
D5	D2	7DH
D6	D1	7EH
D7	D0	7FH



MX	SEG1	SEG2	SEG3	SEG4	SEG5	SEG6	SEG7	SEG8		SEG236	SEG237	SEG238	SEG239	SEG240
0														
1	SEG240	SEG239	SEG238	SEG237	SEG236	SEG235	SEG234	SEG233		SEG5	SEG4	SEG3	SEG2	SEG1

MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=0	MY=1 SL=16	MY=1 SL=16
COM1	COM113	COM128	COM96	COM16	--
COM2	COM114	COM127	COM95	COM15	--
COM3	COM115	COM126	COM94	COM14	--
COM4	COM116	COM125	COM93	COM13	--
COM5	COM117	COM124	COM92	COM12	--
COM6	COM118	COM123	COM91	COM11	--
COM7	COM19	COM122	COM90	COM10	--
COM8	COM120	COM121	COM89	COM9	--
COM9	COM121	COM120	COM88	COM8	--
COM10	COM122	COM119	COM87	COM7	--
COM11	COM123	COM118	COM86	COM6	--
COM12	COM124	COM117	COM85	COM5	--
COM13	COM125	COM116	COM84	COM4	--
COM14	COM126	COM115	COM83	COM3	--
COM15	COM127	COM114	COM82	COM2	--
COM16	COM128	COM113	COM81	COM1	--
COM17	COM1	COM112	COM80	COM128	--
COM18	COM2	COM111	COM79	COM127	--
COM19	COM3	COM110	COM78	COM126	--
COM20	COM4	COM109	COM77	COM125	--
COM21	COM5	COM108	COM76	COM124	--
COM22	COM6	COM107	COM75	COM123	--
COM23	COM7	COM106	COM74	COM122	--
COM24	COM8	COM105	COM73	COM121	--
COM25	COM9	COM104	COM72	COM120	COM96
COM26	COM10	COM103	COM71	COM119	COM95
COM27	COM11	COM102	COM70	COM118	COM94
COM28	COM12	COM101	COM69	COM117	COM93
COM29	COM13	COM100	COM68	COM116	COM92
COM30	COM14	COM99	COM67	COM115	COM91
COM31	COM15	COM98	COM66	COM114	COM90
COM32	COM16	COM97	COM65	COM113	COM89
COM113	COM97	COM16	--	COM32	--
COM114	COM98	COM15	--	COM31	--
COM115	COM99	COM14	--	COM30	--
COM116	COM100	COM13	--	COM29	--
COM117	COM101	COM12	--	COM28	--
COM118	COM102	COM11	--	COM27	--
COM19	COM103	COM10	--	COM26	--
COM120	COM104	COM9	--	COM25	--
COM121	COM105	COM8	--	COM24	--
COM122	COM106	COM7	--	COM23	--
COM123	COM107	COM6	--	COM22	--
COM124	COM108	COM5	--	COM21	--
COM125	COM109	COM4	--	COM20	--
COM126	COM110	COM3	--	COM19	--
COM127	COM111	COM2	--	COM18	--
COM128	COM112	COM1	--	COM17	--
		128	96	128	96
		MUX			

Example for memory mapping: let MX = 0, MY = 0, SL = 0, MSF = 0, according to the data shown in the above table:

⇒ Page 0 SEG 1: 00011110b
⇒ Page 0 SEG 2: 01111000b

TIMING CHARACTERISTICS OF COMPATIBLE CONTROLLER CHIPS

AC CHARACTERISTICS

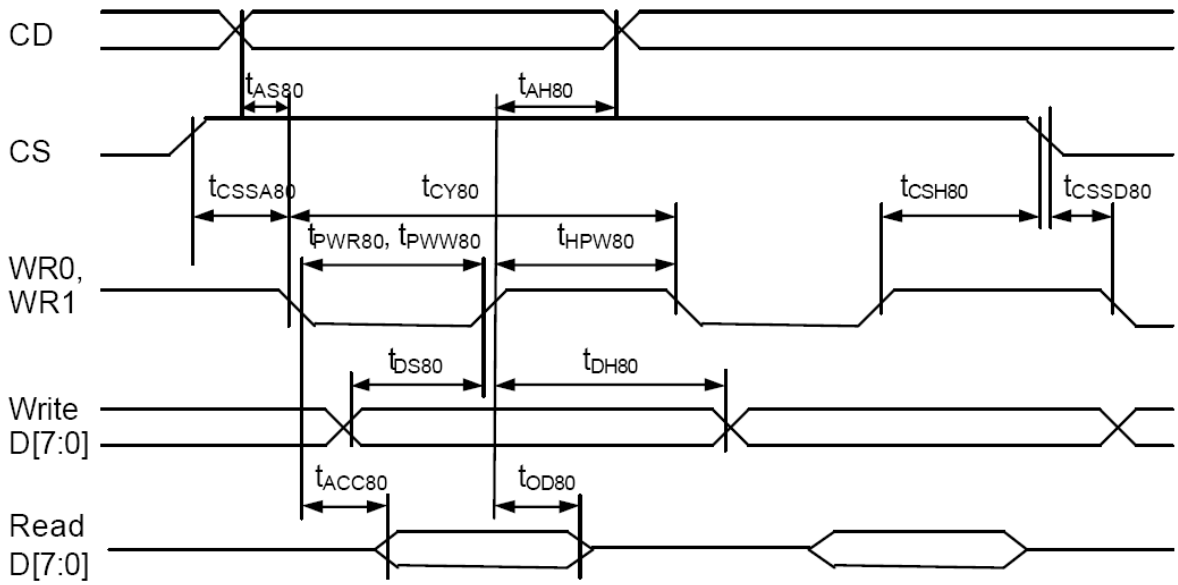


FIGURE 15: Parallel Bus Timing Characteristics (for 8080 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80}	CD	Address setup time		0	–	nS
t_{AH80}		Address hold time		20		
t_{CY80}		System cycle time			–	nS
		8 bits bus (read)		140		
		(write)		140		
		4 bits bus (read)		140		
		(write)		140		
t_{PWR80}	WR1	Pulse width 8 bits (read)		65	–	nS
		4 bits		65		
t_{PWW80}	WR0	Pulse width 8 bits (write)		35	–	nS
		4 bits		35		
t_{HPW80}	WR0, WR1	High pulse width			–	nS
		8 bits bus (read)		65		
		(write)		35		
		4 bits bus (read)		65		
		(write)		35		
t_{DS80}	D0~D7	Data setup time		30	–	nS
t_{DH80}		Data hold time		20		
t_{ACC80}		Read access time	C_L = 100pF	–	60	nS
t_{OD80}		Output disable time		12	20	
t_{SSA80}	CS1/CS0	Chip select setup time		10		nS
t_{CSSD80}				10		
t_{CSH80}				20		

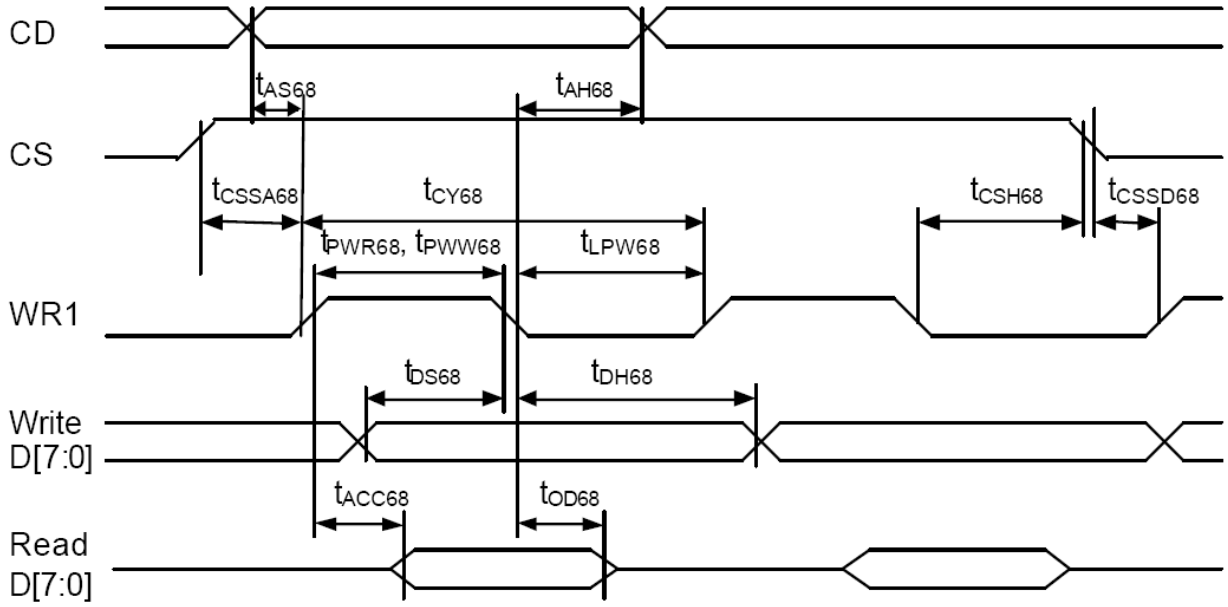


FIGURE 16: Parallel Bus Timing Characteristics (for 6800 MCU)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 20	–	nS
T_{CY68}		System cycle time 8 bits bus (read) (write) 4 bits bus (read) (write)		 140 140 140 140	–	nS
t_{PWR68}	WR1	Pulse width 8 bits (read) 4 bits		65 65	–	nS
t_{PWW68}		Pulse width 8 bits (write) 4 bits		35 35	–	nS
t_{LPW68}		Low pulse width 8 bits bus (read) (write) 4 bits bus (read) (write)		 65 35 65 35	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 20	–	nS
t_{ACC68} t_{OD68}		Read access time Output disable time	C_L = 100pF	– 12	60 20	nS
t_{CSSA68} t_{CSSD68} t_{CSH68}	CS1/CS0	Chip select setup time		10 10 20		nS

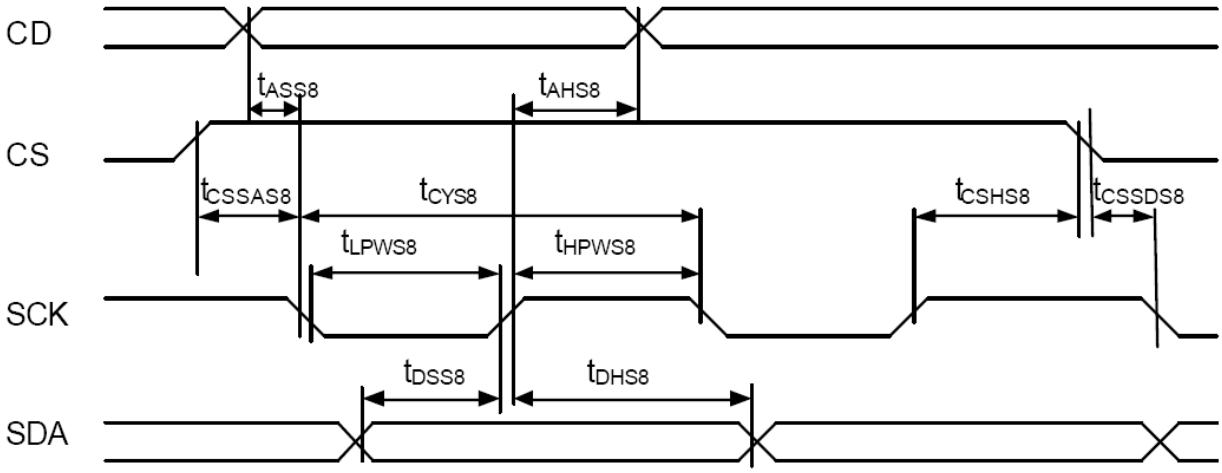


FIGURE 17 : Serial Bus Timing Characteristics (for S8)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		20	–	nS
t_{CYS8}	SCK	System cycle time		140	–	nS
t_{LPWS8}		Low pulse width		65	–	nS
t_{HPWS8}		High pulse width		65	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS8} t_{CSSDS8} t_{CSHS8}	CS	Chip select setup time		10 20 10		nS

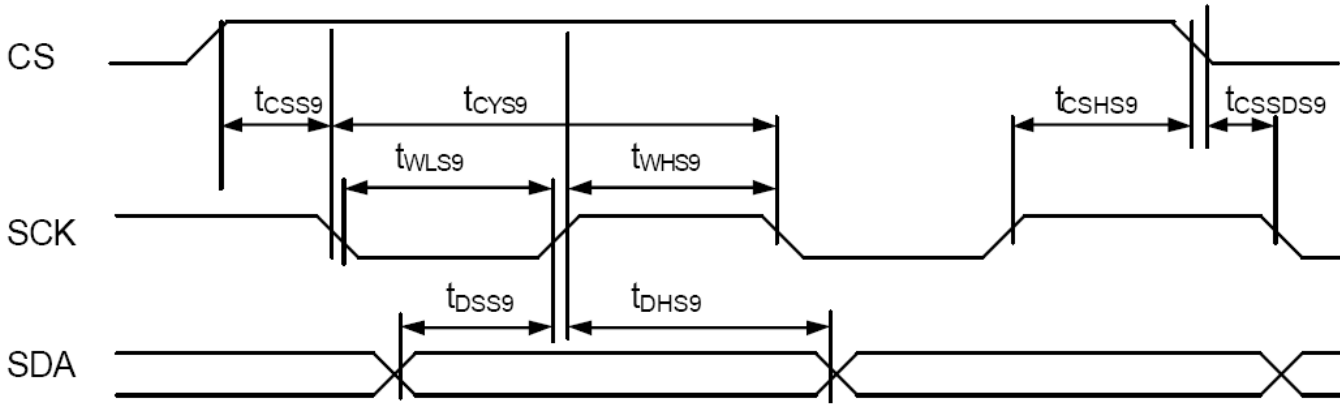


FIGURE 18 : Serial Bus Timing Characteristics (for S9)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYS9}	SCK	System cycle time		140	–	nS
t_{LPWS9}		Low pulse width		65	–	nS
t_{HPWS9}		High pulse width		65	–	nS
t_{DSS9} t_{DHS9}	SDA	Data setup time Data hold time		30 20	–	nS
t_{CSSAS9} t_{CSSDS9} t_{CSHS9}	CS	Chip select setup time		10 20 10		nS

RESET TIMING

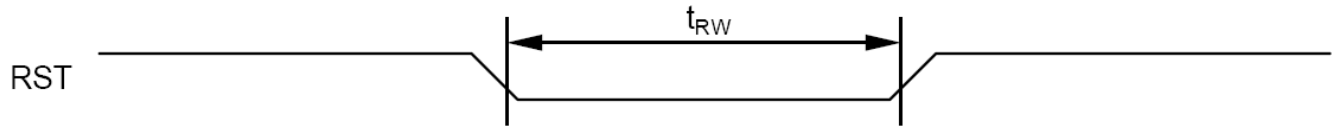


FIGURE 19 : Reset Characteristics

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		1000	–	nS

INITIALIZATION METHOD

POWER-UP

Type	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Chip action	Comments
R	–	–	–	–	–	–	–	–	–	–	Automatic Power-ON-Reset.	Wait 15mS after V_{DD} is ON
C	0	0	0	0	1	0	0	#	#	#	(5) Set MR and TC	
C	0	0	1	1	0	0	#	#	#	#	(15) Set LCD Mapping	Set up LCD specific parameters such as format, MX, MY, MSF, etc.
C	0	0	1	1	1	0	1	0	#	#	(18) Set Bias Ratio	
R	0 0	0 0	1 #	0 #	0 #	0 #	0 #	0 #	0 #	1 #	(9) Set Gain & PM	
C	1 . . 1	0 . . 0	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	# . . #	Write display RAM	Set up display image
R	0	0	1	0	1	0	1	1	1	1	(13) Set Display Enable	

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = VOP / 64 Hz
TEMPERATURE = 23 ± 5 °C
RELATIVE HUMIDITY = 60 ± 20 %

ITEM	SYMBOL	UNIT	TYP. TN	TYP. STN
RESPONSE TIME	Ton	ms	-	290
	Toff	ms	-	370
CONTRAST RATIO	Cr	-	-	9
VIEWING ANGLE (Cr ≥ 2)	V3:00	°	-	40
	V6:00	°	-	60
	V9:00	°	-	40
	V12:00	°	-	40

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

ITEM	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
High temperature operating	50°C	70°C	240 hours
Low temperature operating	0°C	-20°C	240 hours
High temperature storage	60°C	80°C	240 hours
Low temperature storage	-10°C	-30°C	240 hours
Temperature-humidity storage	40°C 90% R.H.	60°C 90% R.H.	96 hours
Temperature cycling	-10°C to 60°C 30 Min Dwell	-30°C to 80°C 30 Min Dwell	5 cycle
Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

QUALITY STANDARD OF LCD MODULE

1.0	**Sampling Method**		
	Sampling Plan : MIL STD 105 E Class of AQL : Level II/Single Sampling Critical : 0.25% Major 0.65% Minor 1.5%		
2.0	**Defect Group**	**Failure Category**	**Failure Reasons**
	Critical Defect 0.25%(AQL)	Malfunction	Open Short Burnt or dead component Missing part/improper part P.C.B. Broken
	Major Defect 0.65%(AQL)	Poor Insulation	Potential short High current Component damage or scratched or Lying too close improper coating
		Poor Conduction	Damage joint Wrong polarity Wrong spec. part Uneven/intermittent contact Loose part Copper peeling Rust or corrosion or dirt‘s
	Minor Defect 1.5%(AQL)	Cosmetic Defect	Minor scratch Flux residue Thin solder Poor plating Poor marking Crack solder Poor bending Poor packing Wrong size

SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

QUALITY STANDARD

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 4 W	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 4 T	MINOR	1
BUBBLES	d* ≥ 0.2 QTY=0	MINOR	2
BLACKS SPOTS	d ≤ 0.3 N.A.** 0.3<d≤0.4 QTY≤1 0.4<d QTY=0	MINOR	2
LINE SCRATCHES	x≥0.7 y≥0.05 QTY=0	MINOR	3
BLACK LINE	x≥0.7 y≥0.05 QTY=0	MINOR	3

*d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : B

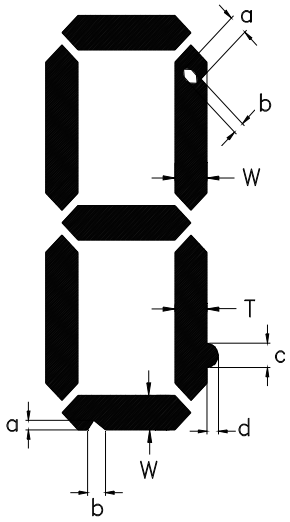
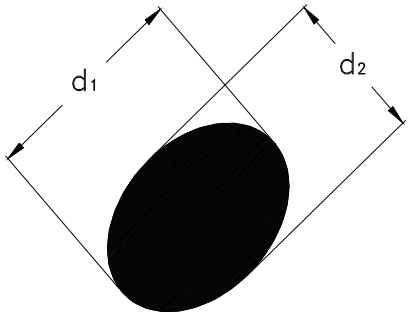
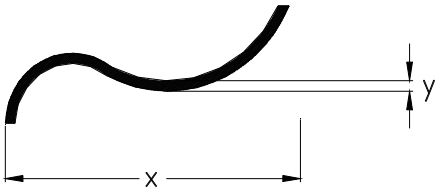


fig . 1



POLARIZER BUBBLES / SPOTS
fig . 2



LINE SCRATCHES / BLACK LINE
fig . 3

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤1/2T f≤1/3W g≤3.5	MINOR	4
	BOTTOM GLASS	p≤1.0 q≤3.5 r≤1/2T		4
	CORNER	a≤1.5 b≤W		4
	TOP GLASS	a≤3.0 b≤1/3T c≤1/2W		5
GLASS PROTRUSION		a ≤ 1/4 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : B

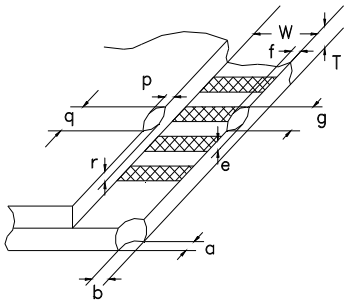


fig . 4

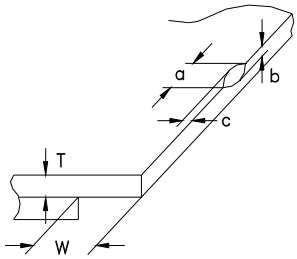


fig . 5

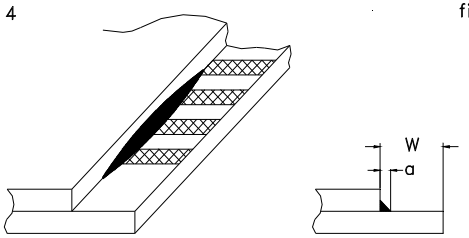


fig . 6

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly.
- Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent;
-water, ketone, aromatics

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to V_{DD} or V_{SS}, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

Remove the protective film slowly and, if possible, under ESD control device like ion blower and humidity of working room should be kept over 50%RH to reduce risk of static charge.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

(4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

(5) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

WARRANTY

CLOVER will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover is limited to repair and/or replacement. Clover will not be responsible for any subsequent or consequential event.