CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model : CG128128A - _ _ - _ _ - _ _ - _

Revision	00
Engineering	Timmy
Date	20 July 2011
Our Reference	X9044

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MODE OF DISPLAY

Display mode	**Display condition**	**Viewing direction**
STN : ☐ Yellow green	☐ Reflective type	☐ 6 O' clock
☐ Grey	☐ Transflective type	☐ 12 O' clock
☐ Blue (negative)	☐ Transmissive type	☐ 3 O' clock
☐ FSTN positive	☐ Others	☐ 9 O' clock
☐ FSTN negative		

LCD MODULE NUMBER NOTATION:

CG128128A- N N - S R - N 6 – T
(1) (2) (3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
T – TN
V – TN (Negative)
S – STN Yellow green
G – STN Grey
B – STN Blue (Negative)
F – FSTN
N – FSTN (Negative)
*(5)---Rear polarizer type
R – Reflective
F – Transflective
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)

GENERAL DESCRIPTION

Display mode : 128 X 128 dots, Graphic COG LCD module

Interface : 8-bit parallel / serial / I^2C

Driving method : 1/128 duty, 1/12 bias

Controller IC : UC1617w or equivalent
For the detailed information, please refer to the IC specifications.

MECHANICAL DIMENSIONS

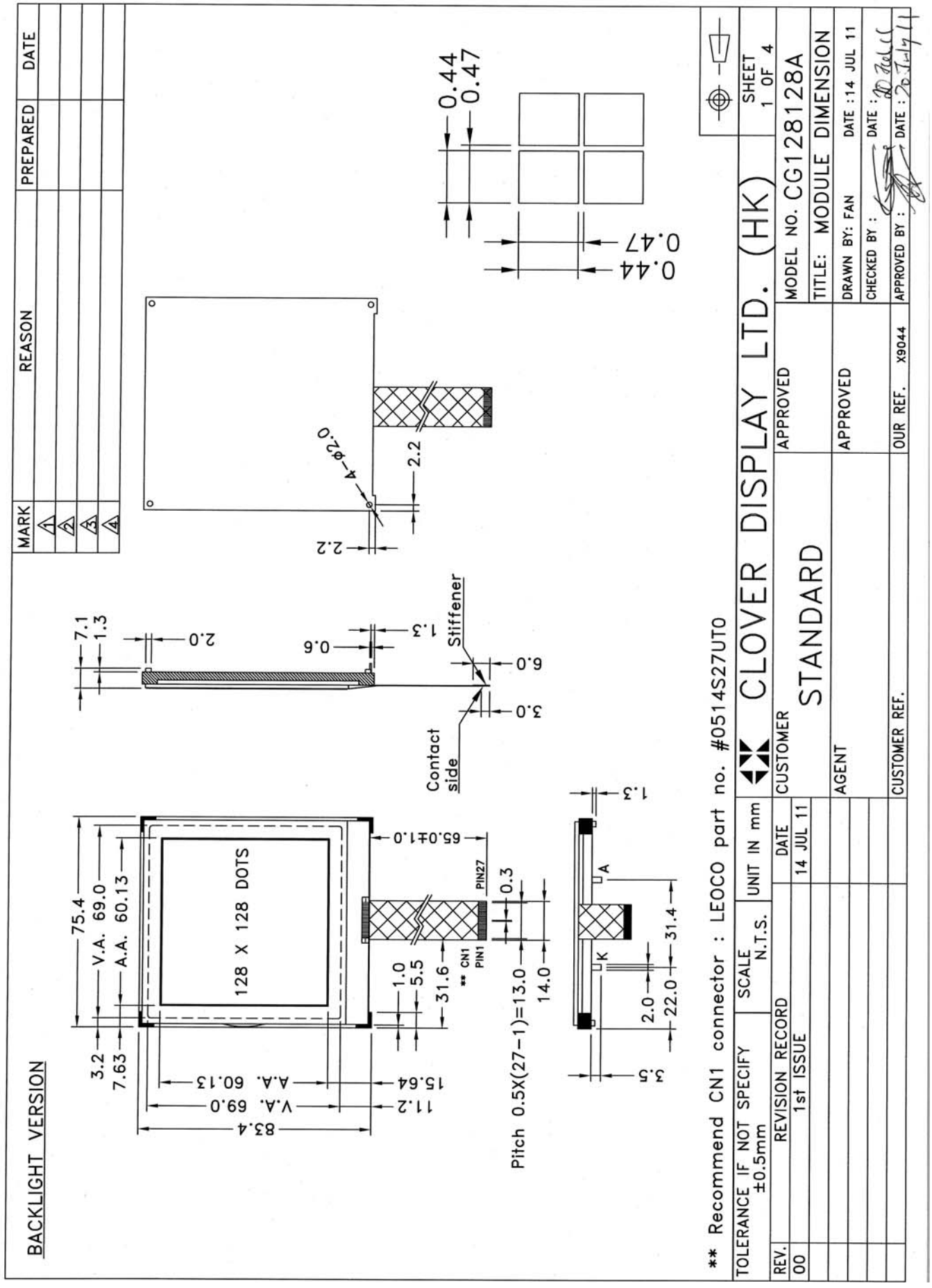
Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension		mm	Viewing Area	69.0(L)x69.0(W)	mm
No Backlight	73.0(L) x 81.0(W) x 2.9MAX.(H)	mm	Dot pitch	0.47(L)x0.47(W)	mm
LED Sided Backlight	75.4(L) x 83.4(W) x 7.1(H)	mm	Dot size	0.44(L)x0.44(W)	mm

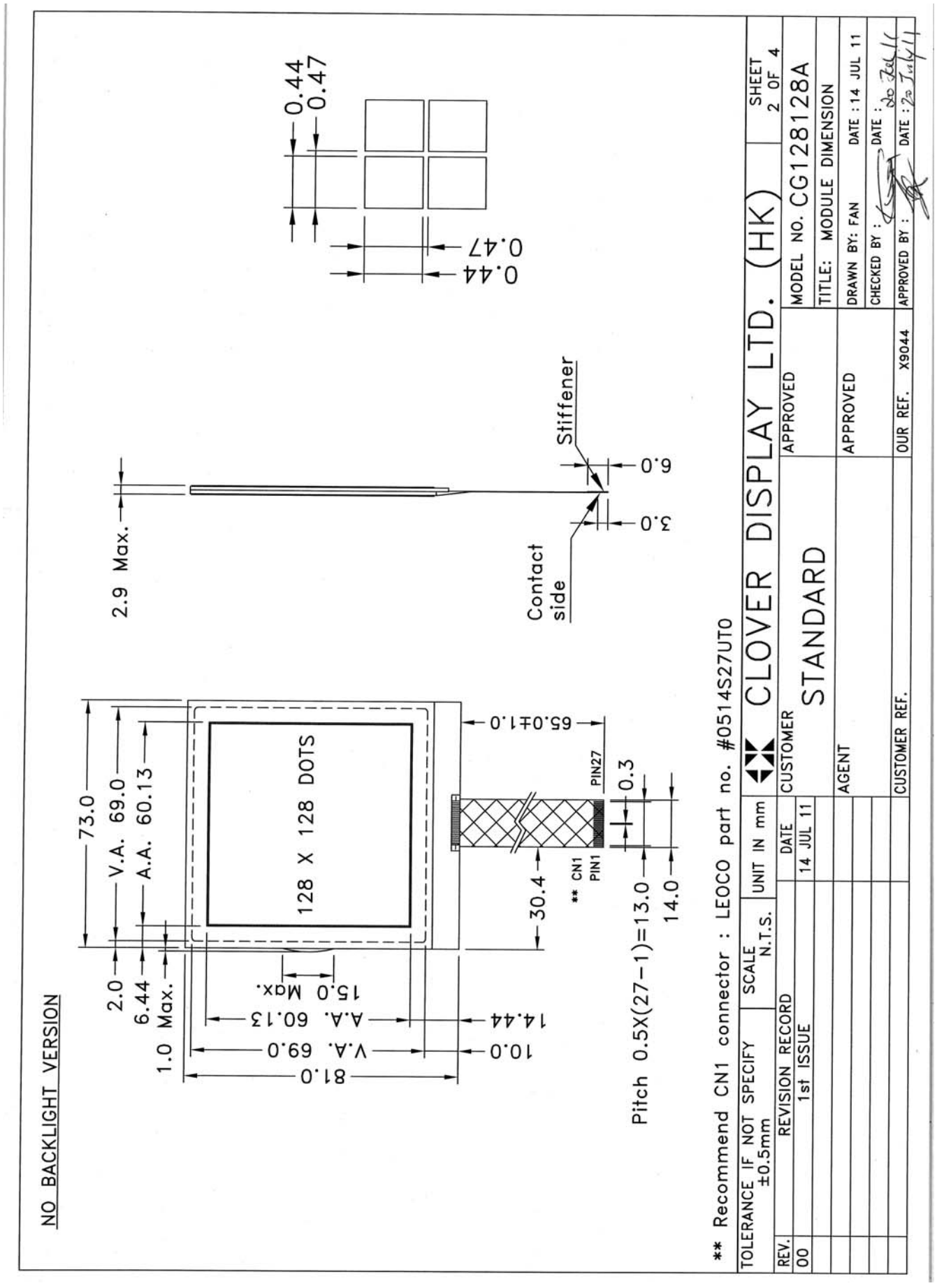
CONNECTOR PIN ASSIGNMENT

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	NC	No connect	15	WR1	Read/write operation control
2	NC	No connect	16	WR0	
3	NC	No connect	17	CD	Register select
4	VLCD	Supply voltage for LCD	18	CS0	Chip select
5	VB0-	LCD bias voltages	19	RST	Reset
6	VB1-		20	D7	Data bus
7	VB1+		21	D6	
8	VB0+		22	D5	
9	VDD	Supply voltage for logic	23	D4	
10	VSS	Ground	24	D3	
11	ID1	Production control	25	D2	
12	ID0		26	D1	
13	BM1	Bus mode select	27	D0	
14	BM0		*28	A	Supply voltage for backlight (+VE)
			*29	K	Supply voltage for backlight (-VE)

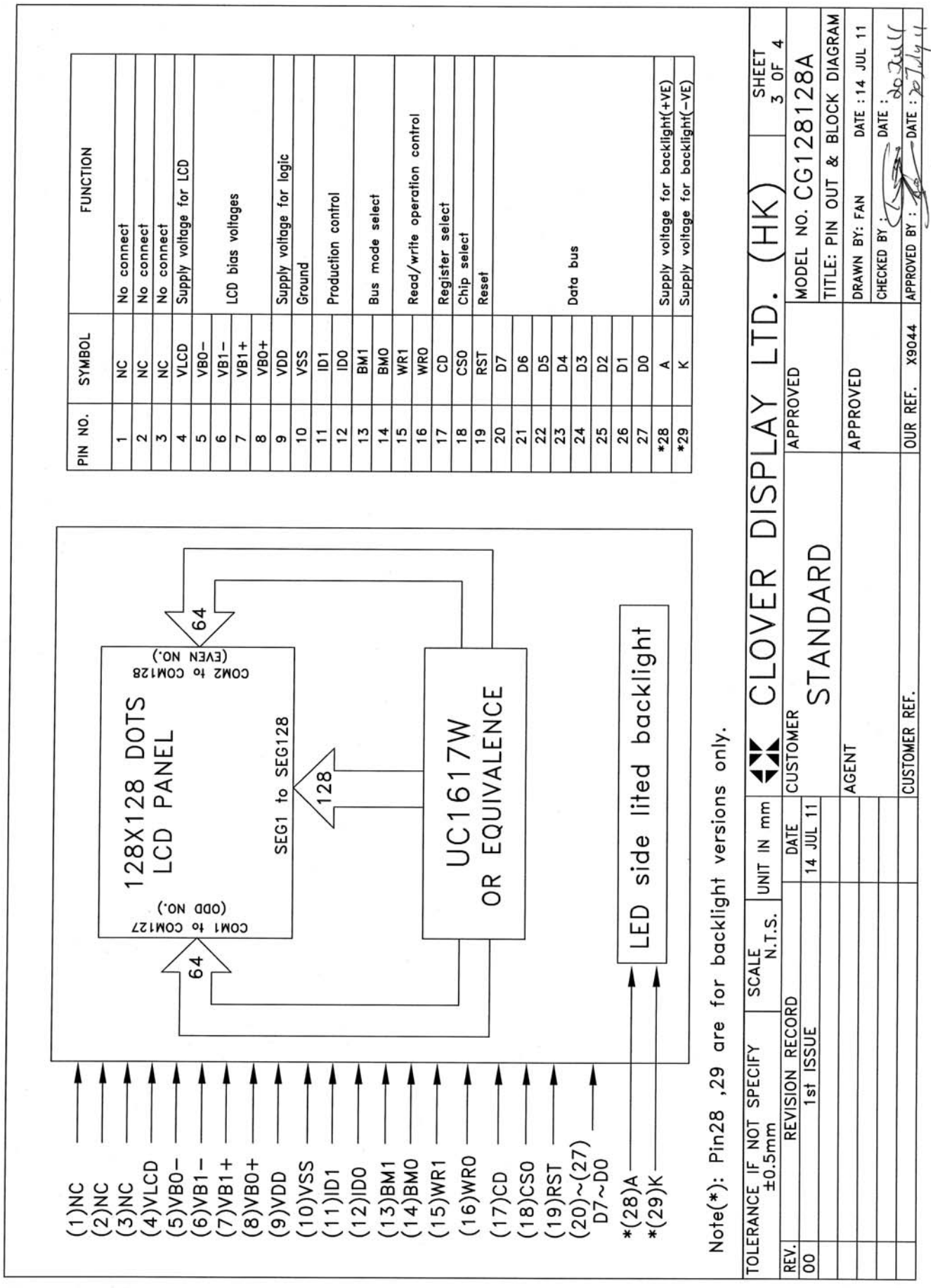
Note (*) : Pin 28, 29 are for backlight versions only.

COUNTER DRAWING OF MODULE DIMENSION




NO BACKLIGHT VERSION
73.0
V.A. 69.0
A.A. 60.13
2.0
6.44
1.0 Max.
128 X 128 DOTS
15.0 Max.
A.A. 60.13
V.A. 69.0
81.0
14.44
10.0
65.0±1.0
PIN27
0.3
30.4
** CN1
PIN1
Pitch 0.5X(27-1)=13.0
14.0
2.9 Max.
Stiffener
0.9
3.0
Contact side
0.44
0.47
0.47
0.44
** Recommend CN1 connector : LEOCO part no. #0514S27UT0
CLOVER DISPLAY LTD. (HK)
SHEET 2 OF 4
TOLERANCE IF NOT SPECIFY ±0.5mm
SCALE N.T.S.
UNIT IN mm
CUSTOMER
APPROVED
MODEL NO. CG128128A
STANDARD
TITLE: MODULE DIMENSION
AGENT
APPROVED
DRAWN BY: FAN DATE : 14 JUL 11
CHECKED BY : DATE :
CUSTOMER REF.
OUR REF. X9044
APPROVED BY : DATE :
REV. REVISION RECORD DATE
00 1st ISSUE 14 JUL 11

COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage for Logic	VDD	3.05	3.3	3.55	V
Supply Current for Logic	IDD	–	1.50	2.25	mA
Operating Voltage for LCD (*)	VLCD	11.8	12.5	13.1	V
'High' Level Input Voltage	VIH	0.8VDD	–	–	V
'Low' Level Input Voltage	VIL	–	–	0.2VDD	V

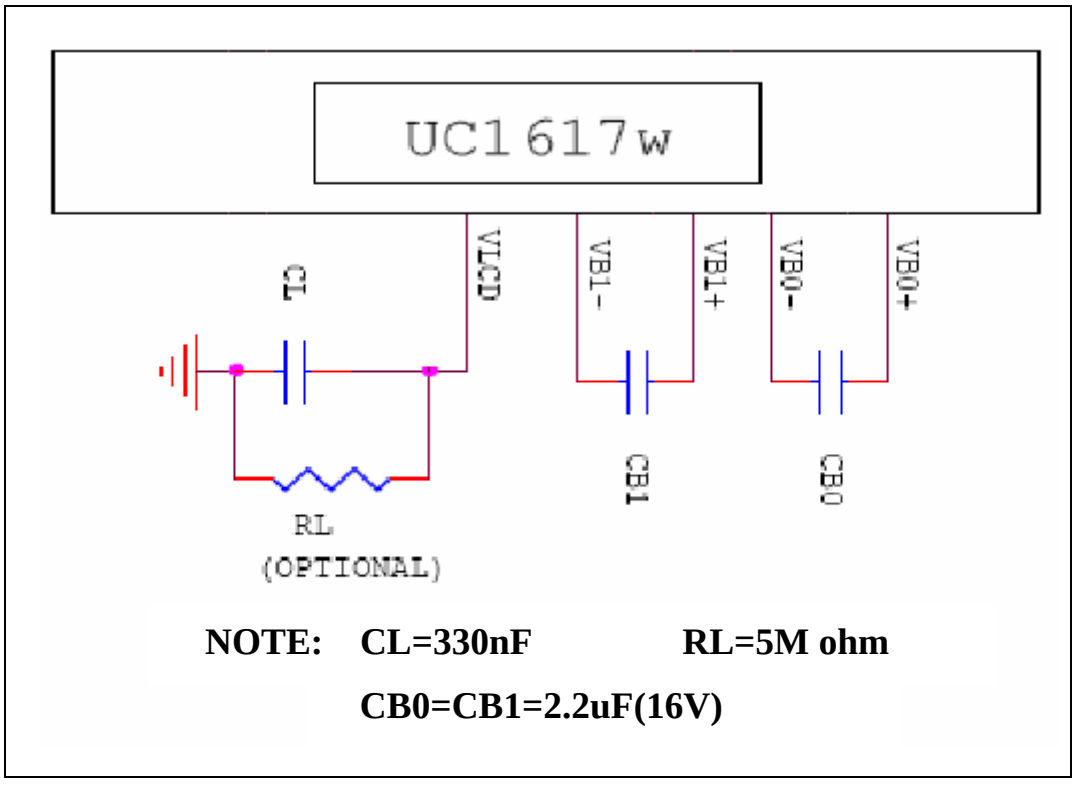
Note (*): There is tolerance in optimum LCD driving voltage during production and it will be within the specified range.

Side-lited LED backlight

Constant voltage driving:

Item	Symbol	MIN.	TYP.	MAX.	Unit	Condition
White color	I_{BL}	–	60	80	mA	V_{BL} = 3.3V
Blue color	I_{BL}	–	60	80	mA	V_{BL} = 3.3V

REFERENCE CIRCUIT EXAMPLE



ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage	VDD	-0.3to4	-0.3to4	V
Input Voltage	VT	-0.4 to VDD +0.5	-0.4 to VDD +0.5	V
Operating Temperature	Topr	0 to 50	-20 to 70	℃
Storage Temperature	Tstg	-10 to 60	-30 to 80	℃

INSTRUCTIONS TABLE

COMMAND SUMMARY

The following is a list of host commands supported by UC1617w

C/D: 0: Control, 1: Data
W/R: 0: Write Cycle, 1: Read Cycle

\# Useful Data bits
– Don't Care

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action	Default
1	Write Data Byte	1	0	#	#	#	#	#	#	#	#	Write 1 byte	N/A
2	Read Data Byte	1	1	#	#	#	#	#	#	#	#	Read 1 byte	N/A
3	Get Status	0	1	1	MX	MY	WA	DE	WS	MD	MS	Get {Status, Ver, PMO, Product Code, PID, MID}	N/A
				Ver		PMO[5:0]							
				Product Code				PID		MID			
4	Set Page_C Address	0	0	0	0	0	#	#	#	#	#	Set CA[4:0]	0H
5	Set Temp. Compensation	0	0	0	0	1	0	0	1	#	#	Set TC[1:0]	00b
6	Set Panel Loading	0	0	0	0	1	0	1	0	#	#	Set PC[1:0]	10b
7	Set Pump Control	0	0	0	0	1	0	1	1	#	#	Set PC[3:2]	11b
8	Set Adv. Program Control	0	0	0	0	1	1	0	0	R	R	Set APC[R][7:0], R = 0, 1 or 2	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
9	Set Scroll Line LSB	0	0	0	1	0	0	#	#	#	#	Set SL[3:0]	0H
	Set Scroll Line MSB	0	0	0	1	0	1	-	#	#	#	Set SL[6:4]	0H
10	Set Row Address LSB	0	0	0	1	1	0	#	#	#	#	Set RA[3:0]	00H
	Set Row Address MSB	0	0	0	1	1	1	-	#	#	#	Set RA[6:4]	00H
11	Set V_{BIAS} Potentiometer	0	0	1	0	0	0	0	0	0	1	Set PM[7:0]	4EH
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
12	Set Partial Display Control	0	0	1	0	0	0	0	1	#	#	Set LC[9:8]	00b: Disable
13	Set RAM Address Control	0	0	1	0	0	0	1	#	#	#	Set AC[2:0]	001b
14	Set Fixed Lines	0	0	1	0	0	1	0	0	0	0	Set {FLT, FLB}	0
				#	#	#	#	#	#	#	#		
15	Set Line Rate	0	0	1	0	1	0	0	0	#	#	Set LC[4:3]	00b
16	Set All-Pixel-ON	0	0	1	0	1	0	0	1	0	#	Set DC[1]	0b
17	Set Inverse Display	0	0	1	0	1	0	0	1	1	#	Set DC[0]	0b
18	Set Display Enable	0	0	1	0	1	0	1	1	#	#	Set DC[3:2]	10b
19	Set LCD Mapping Control	0	0	1	1	0	0	0	#	#	#	Set LC[2:0]	000b
20	Set N-Line Inversion	0	0	1	1	0	0	1	0	0	0	Set NIV[3:0]	6H
				-	-	-	-	#	#	#	#		
21	Set LCD Gray Shade	0	0	1	1	0	1	0	#	#	#	Set LC[7:5]	001b
22	System Reset	0	0	1	1	1	0	0	0	1	0	System Reset	N/A
23	NOP	0	0	1	1	1	0	0	0	1	1	No operation	N/A
24	Set Test Control	0	0	1	1	1	0	0	1	TT		For testing only. Do not use.	N/A
	(double-byte command)	0	0	#	#	#	#	#	#	#	#		
25	Set LCD Bias Ratio	0	0	1	1	1	0	1	0	#	#	Set BR[1:0]	11b: 11
26	Reset Cursor Update Mode	0	0	1	1	1	0	1	1	1	0	AC[3]=0, CA=CR	AC[3]=0
27	Set Cursor Update Mode	0	0	1	1	1	0	1	1	1	1	AC[3]=1, CR=CA	AC[3]=1
28	Set COM End	0	0	1	1	1	1	0	0	0	1	Set CEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		
29	Set Partial Display Start	0	0	1	1	1	1	0	0	1	0	Set DST[6:0]	0
		0	0	-	#	#	#	#	#	#	#		
30	Set Partial Display End	0	0	1	1	1	1	0	0	1	1	Set DEN[6:0]	127
		0	0	-	#	#	#	#	#	#	#		

	Command	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0	Action		Default
31	Set Window Program Starting Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	0 #	0 #	Shared with MTP commands	Set WPC0	0
32	Set Window Programming Starting Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set WPP0	0
33	Set Window Programming Ending Page_C Address	0 0	0 0	1 -	1 -	1 -	1 #	0 #	1 #	1 #	0 #		Set WPC1	31
34	Set Window Programming Ending Row Address	0 0	0 0	1 -	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set WPP1	127
35	Enable window program	0	0	1	1	1	1	1	0	0	#	Set AC[4]		0: Disable
36	Set MTP Operation control	0 0	0 0	1 -	0 -	1 #	1 #	1 #	0 #	0 #	0 #	Set MTPC[5:0]		10H
37	Set MTP Write Mask	0 0	0 0	1 #	0 #	1 #	1 #	1 #	0 #	0 #	1 #	Set MTPM[7:0]		0
38	Set V_{MTP1} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	0 #	Shared with Window Program commands	Set MTP1	N/A
39	Set V_{MTP2} Potentiometer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	0 #	1 #		Set MTP2	
40	Set MTP Write Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	0 #		Set MTP3	
41	Set MTP Read Timer	0 0	0 0	1 #	1 #	1 #	1 #	0 #	1 #	1 #	1 #		Set MTP4	

Notes:

- Any bit patterns other than the commands listed above may result in undefined behavior.
- The interpretation of commands (37)~(41) depends on register MTPC[3].
- Commands (38)~(41) are shared with commands (31)~(34) and have exactly the same code.
  When MTPC[3]=0, commands (38)~(41) are interpreted as `Window Programming` commands.
  When MTPC[3]=1, they are the `MTP Control` commands.
- MTPM and PM are actually the same register. Only one of the commands (37 or 11) is valid at any time, and it is determined by MTPC[3].
- After MTP-ERASE or MTP-PROGRAM operation, before resuming normal operation, please always
  a) Remove TST4 power source,
  b) Do a full V_{DD} ON-OFF-ON cycle.

SET PAGE_C ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Page_C Address LSB CA[4:0]	0	0	**0**	**0**	**0**	CA4	CA3	CA2	CA1	CA0

Set SRAM page_c address for read/write access. Each CA corresponds to one individual SEG electrode.

CA value range: **0**~31

SET TEMPERATURE COMPENSATION

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Temperature Comp. TC[1:0]	0	0	**0**	**0**	**1**	**0**	**0**	**1**	TC1	TC0

Set V_{BIAS} temperature compensation coefficient (%-per-degree-C)

Temperature compensation curve definition:

00b= -0.00%/°C 01b= -0.10%/°C 10b= -0.15%/°C 11b= -0.20%/°C

SET PUMP CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Pump Control PC[3:2]	0	0	**0**	**0**	**1**	**0**	**1**	**1**	PC3	PC2

Set PC[3:2] to program the build-in charge pump stages.

Pump control definition:

00b=External V_{LCD} **11b= Internal V_{LCD}** (9X pump, standard)

SET ROW ADDRESS

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Row Address RA [3:0]	0	0	**0**	**1**	**1**	**0**	RA3	RA2	RA1	RA0
Set Row Address RA [6:4]	0	0	**0**	**1**	**1**	**1**	**-**	RA6	RA5	RA4

Set SRAM row Address for read/write access.

Possible value = **0**~127

SET VBIAS POTENTIOMETER

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set V_{BIAS} Potentiometer. PM [7:0]	0	0	**1**	**0**	**0**	**0**	**0**	**0**	**0**	**1**
(Double-byte command)	0	0	PM7	PM6	PM5	PM4	PM3	PM2	PM1	PM0

Program V_{BIAS} Potentiometer (PM[7:0]). See section LCD VOLTAGE SETTING for more detail.

Effective range: **0 ~ 193**

SET RAM ADDRESS CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set AC [2:0]	0	0	**1**	**0**	**0**	**0**	**1**	AC2	AC1	AC0

Program registers AC[2:0] for RAM address control.

AC[0]: WA, Automatic page_c/row wrap around.
0: CA or RA (depends on AC[1]= 0 or 1) will stop increasing after reaching boundary
1: CA or RA (depends on AC[1]= 0 or 1) will restart, and RA or CA will increase by one.

AC[1]: Auto-Increment order
0 : page_c (CA) increase (+1) first until CA reaches CA boundary, then RA will increase by (+/-1).
1 : row (RA) increase (+/-1) first until RA reach RA boundary, then CA will increase by (+1).

AC[2]: RID, Row Address (RA) auto increment direction (**0**/1 = +/- 1)
When WA=1 and CA reaches CA boundary, PID controls whether row Address will be adjusted by +1 or -1.

AC[2:0] controls the auto-increment behavior of CA and RA. When Window Program is enabled (AC[4]=ON), see Command Description (31) ~ (35) for more details. When Window Program is disabled (AC[4]=OFF), the behavior of CA, RA auto-increment is the same as WPC[1:0] and WPP[1:0] values are the default values and AC[4]=ON.

SET LINE RATE

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Line Rate LC [4:3]	0	0	**1**	**0**	**1**	**0**	**0**	**0**	LC4	LC3

Program LC [4:3] for line rate setting (Line-Rate = Frame-Rate * Mux-Rate). The line rate is automatically scaled down by 2/3, 1/2, 1/3 and 1/4 at Mux-Rate = 85, 64, 43, and 32.

The followings are line rates at Mux Rate = 86~128:

00b: 14.2 Klps 01b: 17.3 Klps 10b: 21.1 Klps 11b: 25.7 Klps
(Klps: Kilo-Line-per-second)

while the followings are line rates in On/Off mode:

00b: 5.7 Klps 01b: 7.0 Klps 10b: 8.5 Klps 11b: 10.4 Klps

SET LCD MAPPING CONTROL

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set LCD Mapping Control LC [2:0]	0	0	**1**	**1**	**0**	**0**	**0**	MY	MX	LC0

This command is used for programming LC[2:0] for COM (row) mirror (MY), SEG (page_c) mirror (MX).

LC2 controls Mirror Y (MY): MY is implemented by reversing the mapping order between RAM and COM electrodes. The data stored in RAM is not affected by MY command. MY will have immediate effect on the display image.

LC1 controls Mirror X (MX): MX is implemented by selecting the CA or 31-CA as write/read (from host interface) display RAM page_c address so this function will only take effect after rewriting the RAM data.

LC0 controls whether the soft icon section (0~ 2xFL) is display or not during partial display mode.

SYSTEM RESET

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
System Reset	0	0	**1**	**1**	**1**	**0**	**0**	**0**	**1**	**0**

This command will activate the system reset. Control register values will be reset to their default values. Data stored in RAM will not be affected.

SET LCD BIAS RATIO

Action	C/D	W/R	D7	D6	D5	D4	D3	D2	D1	D0
Set Bias Ratio BR [1:0]	0	0	**1**	**1**	**1**	**0**	**1**	**0**	BR1	BR0

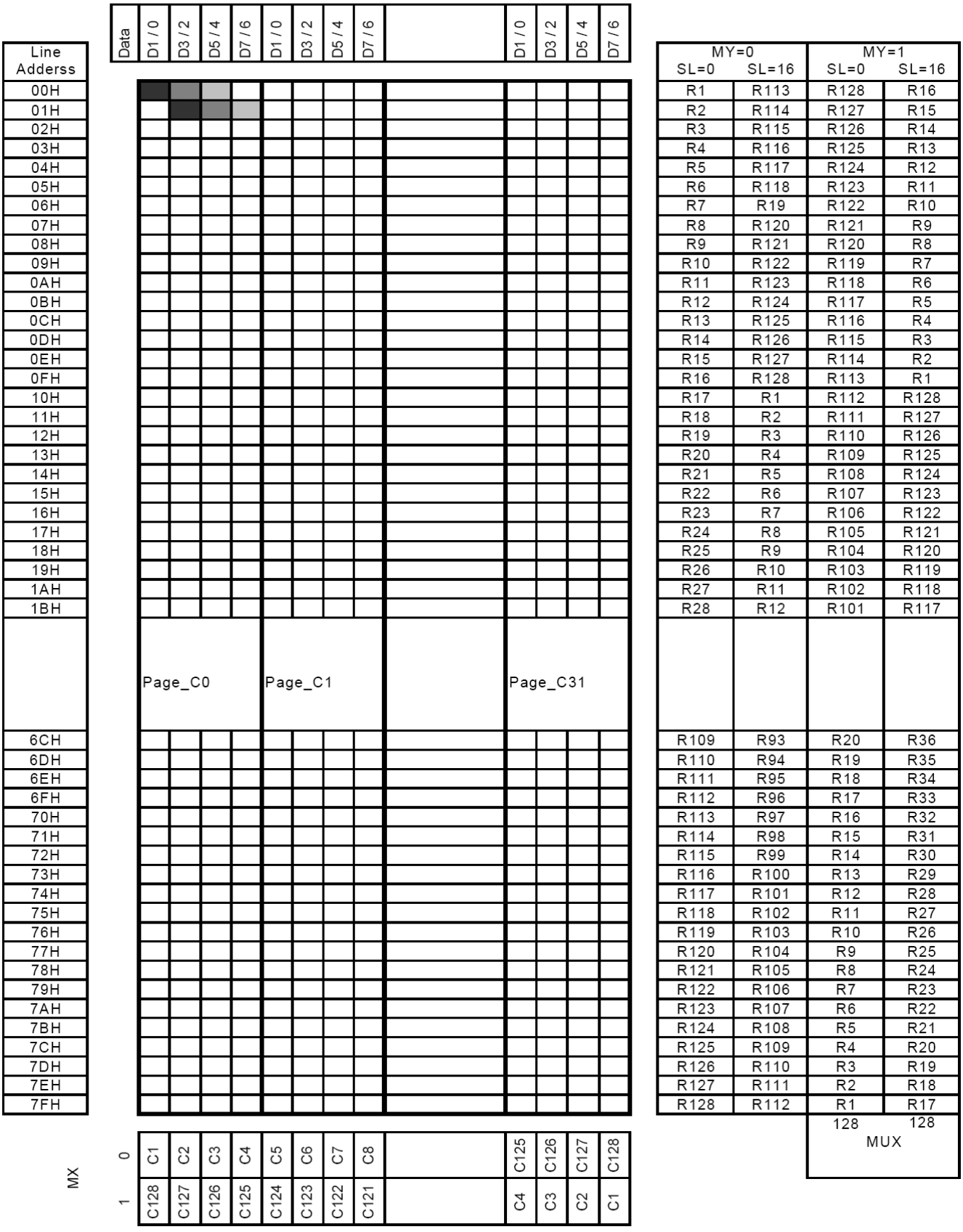
Bias ratio definition:

00b = 6 01b = 9 10b = 10 **11b = 11**

RECOMMENDED INITIAL SETTINGS

System Reset：E2H
Set Temp. compensation：24H
Set Up LCD Format Specific Parameters ,MX,MY,etc：C4H
Set Line Rate：A3H
Set Pump Control：2fH
Set LCD Bias Ratio：EAH
LCD Specific Operation Voltage Setting：81H
Set RAM Address Control：89H
Set Page_C Address：00H
Set Row Address MSB：70H
Set Row Address LSB：60H
Set B/W MODE display enable：ADH

DISPLAY DATA RAM



Line Adderss	MY=0 SL=0	MY=0 SL=16	MY=1 SL=0	MY=1 SL=16
00H	R1	R113	R128	R16
01H	R2	R114	R127	R15
02H	R3	R115	R126	R14
03H	R4	R116	R125	R13
04H	R5	R117	R124	R12
05H	R6	R118	R123	R11
06H	R7	R19	R122	R10
07H	R8	R120	R121	R9
08H	R9	R121	R120	R8
09H	R10	R122	R119	R7
0AH	R11	R123	R118	R6
0BH	R12	R124	R117	R5
0CH	R13	R125	R116	R4
0DH	R14	R126	R115	R3
0EH	R15	R127	R114	R2
0FH	R16	R128	R113	R1
10H	R17	R1	R112	R128
11H	R18	R2	R111	R127
12H	R19	R3	R110	R126
13H	R20	R4	R109	R125
14H	R21	R5	R108	R124
15H	R22	R6	R107	R123
16H	R23	R7	R106	R122
17H	R24	R8	R105	R121
18H	R25	R9	R104	R120
19H	R26	R10	R103	R119
1AH	R27	R11	R102	R118
1BH	R28	R12	R101	R117
6CH	R109	R93	R20	R36
6DH	R110	R94	R19	R35
6EH	R111	R95	R18	R34
6FH	R112	R96	R17	R33
70H	R113	R97	R16	R32
71H	R114	R98	R15	R31
72H	R115	R99	R14	R30
73H	R116	R100	R13	R29
74H	R117	R101	R12	R28
75H	R118	R102	R11	R27
76H	R119	R103	R10	R26
77H	R120	R104	R9	R25
78H	R121	R105	R8	R24
79H	R122	R106	R7	R23
7AH	R123	R107	R6	R22
7BH	R124	R108	R5	R21
7CH	R125	R109	R4	R20
7DH	R126	R110	R3	R19
7EH	R127	R111	R2	R18
7FH	R128	R112	R1	R17
			128	128
			MUX	

Example: when MX=0, MY=0, SL=0, the corresponding data in SRAM as the pixels shown is:

Row1 Page_C0 ⇨ 11100100b

Row2 Page_C0 ⇨ 00111001b

PARALLEL INTERFACE BUS TIMING CHARACTERISTICS FOR 8080 MODE

AC CHARACTERISTICS

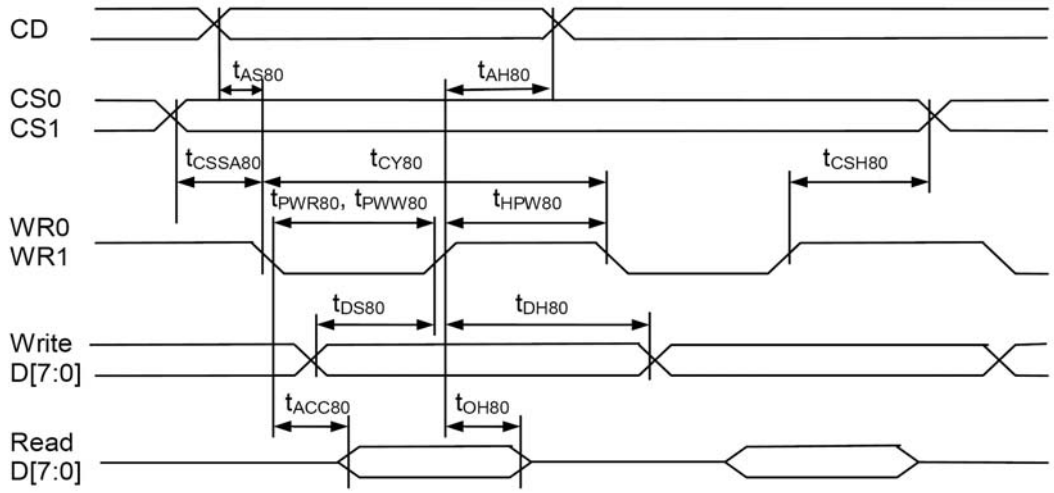


FIGURE 13: Parallel Bus Timing Characteristics (for 8080 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time (read) (write)		170 130	–	nS
t_{PWR80}	WR1	Pulse width (read)		85	–	nS
t_{PWW80}	WR0	Pulse width (write)		65	–	nS
t_{HPW80}	WR0, WR1	High pulse width (read) (write)		85 65	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC80} t_{OH80}		Read access time Output disable time	C_L = 100pF	– –	65 30	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS80} t_{AH80}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY80}		System cycle time (read) (write)		320 270	–	nS
t_{PWR80}	WR1	Pulse width (read)		160	–	nS
t_{PWW80}	WR0	Pulse width (write)		135	–	nS
t_{HPW80}	WR0, WR1	High pulse width (read) (write)		160 135	–	nS
t_{DS80} t_{DH80}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC80} t_{OH80}		Read access time Output disable time	C_L = 100pF	– –	120 60	nS
t_{CSSA80} t_{CSH80}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

PARALLEL INTERFACE BUS TIMING CHARACTERISTICS FOR 6800 MODE

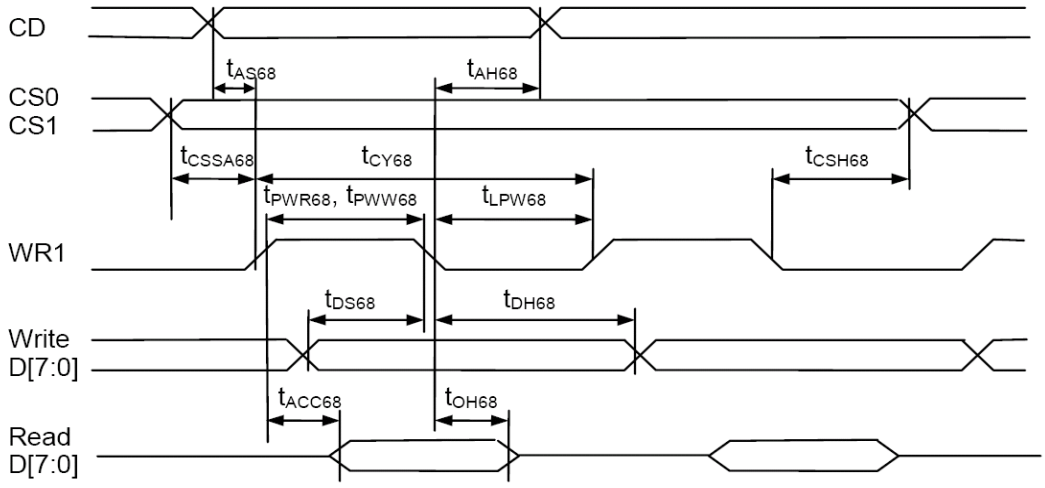


FIGURE 14: Parallel Bus Timing Characteristics (for 6800 MCU)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time (read) (write)		170 130	–	nS
t_{PWR68}	WR1	Pulse width (read)		85	–	nS
t_{PWW68}		Pulse width (write)		65	–	nS
t_{LPW68}		Low pulse width (read) (write)		85 65	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		30 0	–	nS
t_{ACC68} t_{OH68}		Read access time Output disable time	C_L = 100pF	– –	70 30	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{AS68} t_{AH68}	CD	Address setup time Address hold time		0 0	–	nS
t_{CY68}		System cycle time (read) (write)		320 270	–	nS
t_{PWR68}	WR1	Pulse width (read)		160	–	nS
t_{PWW68}		Pulse width (write)		135	–	nS
t_{LPW68}		Low pulse width (read) (write)		160 135	–	nS
t_{DS68} t_{DH68}	D0~D7	Data setup time Data hold time		60 0	–	nS
t_{ACC68} t_{OH68}		Read access time Output disable time	C_L = 100pF	– –	120 60	nS
t_{CSSA68} t_{CSH68}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

SERIAL INTERFACE BUS TIMING CHARACTERISTICS FOR S8 MODE

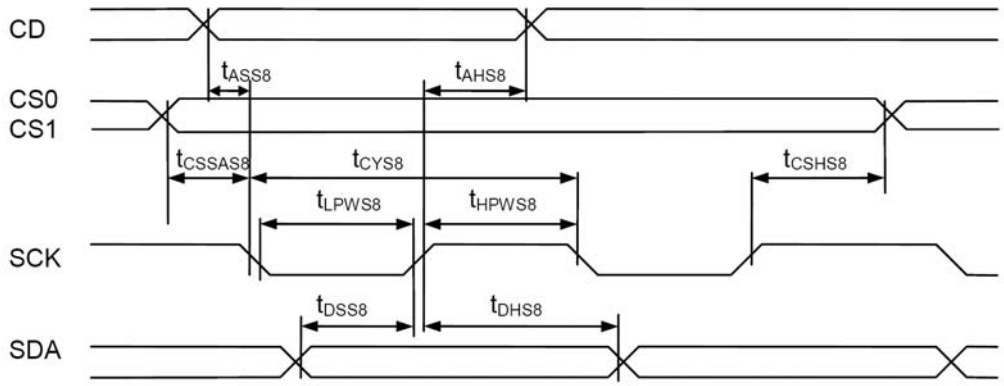


FIGURE 15: Serial Bus Timing Characteristics (for S8 / S8uc)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		40	–	nS
t_{LPWS8}		Low pulse width		20	–	nS
t_{HPWS8}		High pulse width		20	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data disable time		15 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		5 5		nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{ASS8}	CD	Address setup time		0	–	nS
t_{AHS8}		Address hold time		0	–	nS
t_{CYS8}	SCK	System cycle time		75	–	nS
t_{LPWS8}		Low pulse width		37	–	nS
t_{HPWS8}		High pulse width		37	–	nS
t_{DSS8} t_{DHS8}	SDA	Data setup time Data disable time		30 0	–	nS
t_{CSSAS8} t_{CSHS8}	CS1/CS0	Chip select setup time Chip select hold time		10 10		nS

SERIAL INTERFACE BUS TIMING CHARACTERISTICS FOR I2C MODE

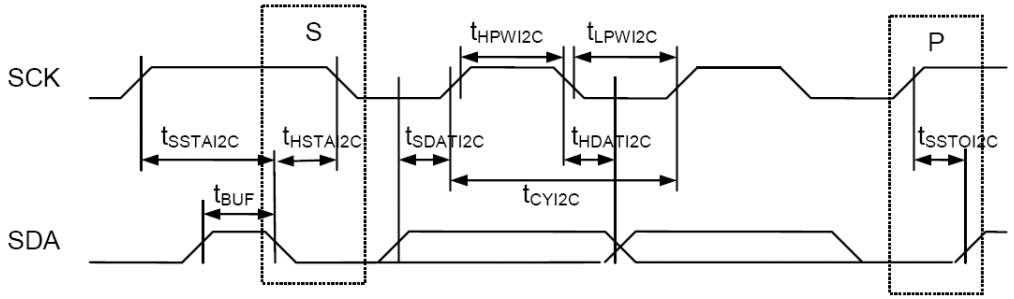


FIGURE 16: Serial bus timing characteristics (for I^2C)

($2.5V \leqslant V_{DD} < 3.3V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ⩽ 100nS	580 275	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		290 165	–	nS
t_{HPWI2C}		High pulse width (read) (write)		290 110	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		28	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		28	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		165	–	nS

($1.65V \leqslant V_{DD} < 2.5V$, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{CYI2C}	SCK	SCK cycle time (read) (write)	tr+tf ⩽ 100nS	750 330	–	nS
t_{LPWI2C}		Low pulse width (read) (write)		375 200	–	nS
t_{HPWI2C}		High pulse width (read) (write)		375 130	–	nS
tr, tf	SCK SDA	Rise time and fall time		–	–	nS
$t_{SSDAI2C}$		Data setup time		55	–	nS
t_{HDAI2C}		Data hold time		11	–	nS
$t_{SSTAI2C}$		START Setup time		28	–	nS
$t_{HSTAI2C}$		START Hold time		60	–	nS
$t_{SSTOI2C}$		STOP setup time		28	–	nS
T_{BUF}		Bus Free time between STOP and START condition		220		nS

RESET TIMING DIAGRAM

FIGURE 17: Reset Characteristics

(1.65V ≤ V_{DD} < 3.3V, Ta= –30 to +85°C)

Symbol	Signal	Description	Condition	Min.	Max.	Units
t_{RW}	RST	Reset low pulse width		3	–	µS
t_{RD}	RST, WR	Reset to WR pulse delay		10	–	mS

THE RESET CIRCUIT

RESET & POWER MANAGEMENT

TYPES OF RESET

UC1617w has two different types of Reset: *Power-ON-Reset* and *System-Reset*.

Power-ON-Reset is performed right after V_{DD} is connected to power. *Power-On-Reset* will first wait for about ~5mS, depending on the time required for V_{DD} to stabilize, and then trigger the *System Reset*.

System Reset can also be activated by software command or by connecting RST pin to ground.

In the following discussions, Reset means *System Reset*.

RESET STATUS

When UC1617w enters RESET sequence:

- Operation mode will be "Reset"
- All control registers are reset to default values. Refer to Control Registers for details of their default values.

OPERATION MODES

UC1617w has three operating modes (OM): Reset, Normal, Sleep.

Mode	Reset	Sleep	Normal
OM	00	10	11
Host Interface	Active	Active	Active
Clock	OFF	OFF	ON
LCD Drivers	OFF	OFF	ON
Charge Pump	OFF	OFF	ON
Draining Circuit	ON	ON	OFF

Table 4: Operating Modes

CHANGING OPERATION MODE

In addition to Power-ON-Reset, two commands will initiate OM transitions: *Set Display Enable*, and *System Reset*.

When DC[2] is modified by *Set Display Enable*, OM will be updated automatically. There is no other action required to enter Sleep Mode.

OM changes are synchronized with the edges of UC1617w internal clock. To ensure consistent system states, wait at least 10µS after `Set Display Enable` *or* `System Reset` commands.

Action	Mode	OM
Reset command RST_ pin pulled "L" Power ON reset	Reset	00
Set Driver Enable to "0"	Sleep	10
Set Driver Enable to "1"	Normal	11

Table 5: OM changes

Both Reset mode and Sleep mode drain the charges stored in the external capacitors C_{B0}, C_{B1}, and C_L. When entering Reset mode or Sleep mode, the display drivers will be disabled.

The difference between Sleep mode and Reset mode is that, Reset mode clears all control registers and restores them to default values, while Sleep mode retains all the control registers values set by the user.

It is recommended to use Sleep Mode for Display OFF operations as UC1617w consumes very little energy in Sleep mode (typically under 2µA).

EXITING SLEEP MODE

UC1617w contains internal logic to check whether V_{LCD} and V_{BIAS} are ready before releasing COM and SEG drivers from their idle states. When exiting Sleep or Reset mode, COM and SEG drivers will not be activated until UC1617w internal voltage sources are restored to their proper values.

INITIALIZING WITHOUT THE BUILT-IN POWER SUPPLY CIRCUITS

POWER-UP SEQUENCE

UC1617w power-up sequence is simplified by built-in "Power Ready" flags and the automatic invocation of `System-Reset` command after *Power-ON-Reset*.

System programmers are only required to wait 150 mS before the CPU starting to issue commands to UC1617w. No additional time sequences are required between enabling the charge pump, turning on the display drivers, writing to RAM or any other commands. However, while turning on V_{DD}, $V_{DD2/3}$ should be started not later than V_{DD}.

Delay allowance between V_{DD} and $V_{DD2/3}$ is illustrated as Figure 12.

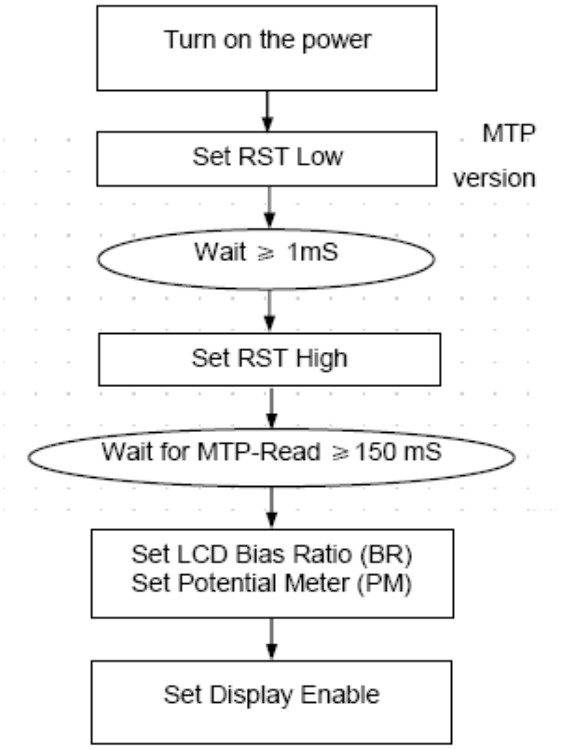


Figure 10: Reference Power-Up Sequence

POWER-DOWN SEQUENCE

To prevent the charge stored in capacitors C_{BX+}, C_{BX-}, and C_L from damaging the LCD, when V_{DD} is switched off, use Reset mode to enable the built-in draining circuit and discharge these capacitors.

The draining resistor is 1K Ohm for both V_{LCD} and V_{B+}. It is recommended to wait *3 x RC* for V_{LCD} and *1.5 x RC* for V_{B+}. For example, if C_L is 330nF, then the draining time required for V_{LCD} is 0.5~1mS.

When internal V_{LCD} is not used, UC1617w will *NOT* drain V_{LCD} during RESET. System designers need to make sure external V_{LCD} source is properly drained off before turning off V_{DD}.

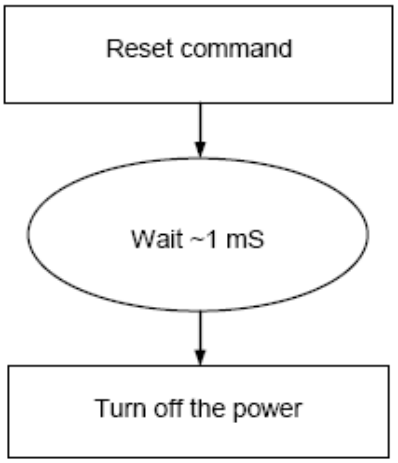


Figure 11: Reference Power-Down Sequence

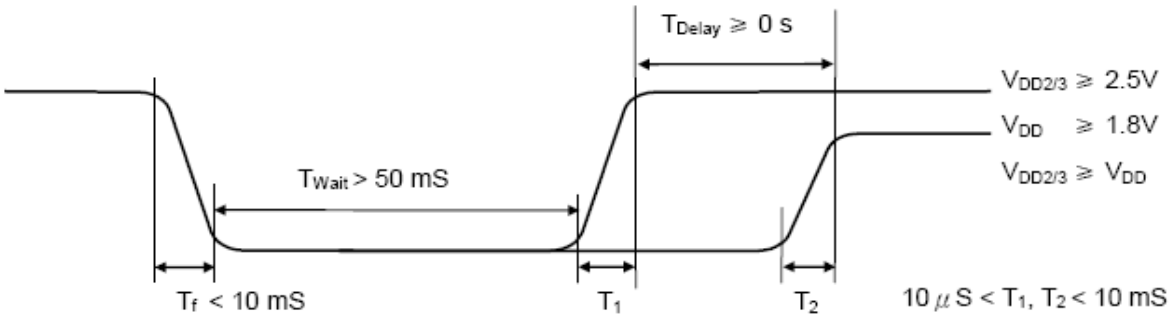


Figure 12: Delay allowance between V_{DD} and V_{DD23}

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = V_{OP} / 64 Hz
TEMPERATURE = 22 ± 5 °C
RELATIVE HUMIDITY = 60 ± 15 %

ITEM	SYMBOL	UNIT	TYP. STN
RESPONSE TIME	Ton	ms	290
	Toff	ms	370
CONTRAST RATIO	Cr	-	9
VIEWING ANGLE (Cr ≥ 2)	$V_{3:00}$	°	40
	$V_{6:00}$	°	60
	$V_{9:00}$	°	40
	$V_{12:00}$	°	40

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

ITEM	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
High temperature operating	50°C	70°C	240 hours
Low temperature operating	0°C	-20°C	240 hours
High temperature storage	60°C	80°C	240 hours
Low temperature storage	-10°C	-30°C	240 hours
Temperature-humidity storage	40°C 90% R.H.	60°C 90% R.H.	96 hours
Temperature cycling	-10°C to 60°C 30 Min Dwell	-30°C to 80°C 30 Min Dwell	5 cycle
Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

QUALITY STANDARD OF LCD MODULE

1.0	**Sampling Method**		
	Sampling Plan : MIL STD 105 E Class of AQL : Level II/Single Sampling Critical : 0.25% Major 0.65% Minor 1.5%		
2.0	**Defect Group**	**Failure Category**	**Failure Reasons**
	Critical Defect 0.25%(AQL)	Malfunction	Open Short Burnt or dead component Missing part/improper part P.C.B. Broken
	Major Defect 0.65%(AQL)	Poor Insulation	Potential short High current Component damage or scratched or Lying too close improper coating
		Poor Conduction	Damage joint Wrong polarity Wrong spec. part Uneven/intermittent contact Loose part Copper peeling Rust or corrosion or dirt‘s
	Minor Defect 1.5%(AQL)	Cosmetic Defect	Minor scratch Flux residue Thin solder Poor plating Poor marking Crack solder Poor bending Poor packing Wrong size

SAMPLING METHOD

SAMPLING PLAN: MIL-STD 105E

CLASS OF AQL: LEVEL II/ SINGLE SAMPLING
MAJOR-0.65% MINOR – 1.5%

QUALITY STANDARD

DEFECT	CRITERIA	TYPE	FIGURE
SHORT CIRCUIT	-	MAJOR	-
MISSING SEGMENT	-	MAJOR	-
UNEVEN / POOR CONTRAST	-	MAJOR	-
CROSS TALK	-	MAJOR	-
PIN HOLE	MAX(a,b) ≤ 1 / 4 W	MINOR	1
EXCESS SEGMENT	MAX(c,d) ≤ 1 / 4 T	MINOR	1
BUBBLES	d* ≥ 0.2 QTY=0	MINOR	2
BLACKS SPOTS	d ≤ 0.3 N.A.** 0.3<d≤0.4 QTY≤1 0.4<d QTY=0	MINOR	2
LINE SCRATCHES	x≥0.7 y≥0.05 QTY=0	MINOR	3
BLACK LINE	x≥0.7 y≥0.05 QTY=0	MINOR	3

*d = MAX (d_1,d_2) ** N. A . = NOT APPLICABLE DEFECT TABLE : B

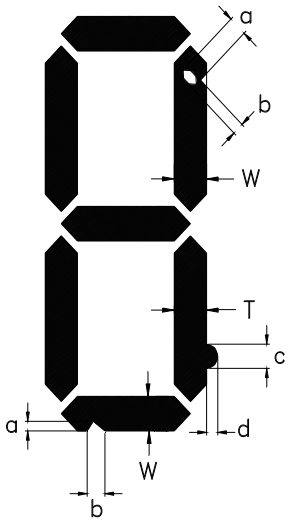
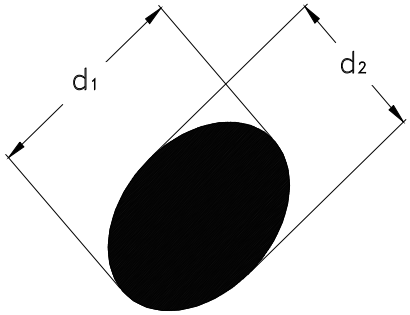
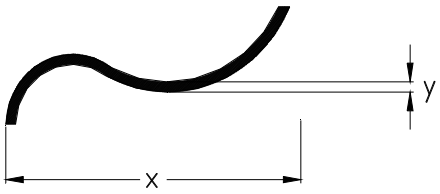


fig . 1



POLARIZER BUBBLES / SPOTS
fig . 2



LINE SCRATCHES / BLACK LINE
fig . 3

QUALITY STANDARD (CONT .)

DEFECT		CRITERIA	TYPE	FIGURE
CHIPS	CONTACT EDGE	e≤1/2T f≤1/3W g≤3.5	MINOR	4
	BOTTOM GLASS	p≤1.0 q≤3.5 r≤1/2T		4
	CORNER	a≤1.5 b≤W		4
	TOP GLASS	a≤3.0 b≤1/3T c≤1/2W		5
GLASS PROTRUSION		a ≤ 1/4 W	MINOR	6
RAINBOW		-	MINOR	-

UNLESS STATE OTHERWISE , ALL UNIT ARE IN MILLIMETER . DEFECT TABLE : B

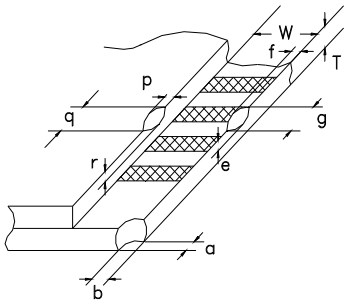


fig . 4

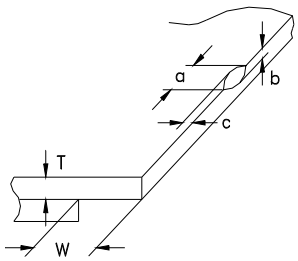


fig . 5

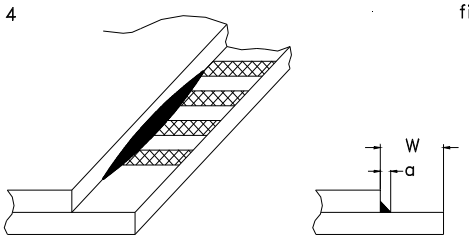


fig . 6

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

Use soft cloth with solvent (recommended below) to clean the display surface and wipe lightly.
- Isopropyl alcohol, ethyl alcohol, trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface. Do not use the following solvent;
-water, ketone, aromatics

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommend that any unused input terminal would be connected to V_{DD} or V_{SS}, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

Remove the protective film slowly and, if possible, under ESD control device like ion blower and humidity of working room should be kept over 50%RH to reduce risk of static charge.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed direct to sunshine or high temperature/humidity.

(4) CAUTION FOR OPERATION

It is an indispensable condition to drive LCD's within the specified voltage limit since the higher voltage than the limit causes the shorter LCD life. The use of direct current drive should be avoided because an electrochemical reaction due to direct current causes LCD's undesirable deterioration.

Response time will be extremely delayed at low temperature, and LCD's show dark color at high temperature. However those phenomena do not mean malfunction or out of order with LCD's.

Some font will be abnormally displayed when the display area is pushed hard during operation. But it resumes normal condition after turning off once.

(5) SOLDERING (for Pin type)

It is recommended to complete dip soldering at 270 ^{o}C or hand soldering at 280 ^{o}C within 3 seconds. The soldering position is at least 3mm apart from the pin head. Wave or reflow soldering are not recommended. Metal pins should not be soldered for more than 3 times and each soldering should be done after cool down of metal pins

(6) SAFETY

For crash damaged or unnecessary LCD's, it is recommended to wash off liquid crystal by either of solvents such as acetone and ethanol and should be burned up later.

When any liquid leaked out of a damaged glass cell comes in contact with your hands, wash it off with soap and water.

WARRANTY

CLOVER will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover is limited to repair and/or replacement. Clover will not be responsible for any subsequent or consequential event.