CLOVER DISPLAY LTD.

LCD MODULE SPECIFICATION

Model: CV320240H - _ _ - _ _ - _ _ -_ _

Revision	00
Engineering	TIMMY
Date	31 October 2009
Our Reference	4935

ADDRESS : ROOM 1006, 10/F WESTIN CENTRE, 26 HUNG TO ROAD, KWUN TONG, KOWLOON, HONG KONG.

TEL : (852) 2341 3238 (SALES OFFICE) (852) 2342 8228 (GENERAL OFFICE)

FAX : (852) 2357 4237 (SALES OFFICE) (852) 2341 8785 (GENERAL OFFICE)

E-MAIL : cdl@cloverdisplay.com

URL : http://www.cloverdisplay.com

MODE OF DISPLAY

Display mode	Display condition	Viewing direction
STN : ☐ Yellow green	☐ Reflective type	☐ 6 O' clock
☐ Grey	☐ Transflective type	☐ 12 O' clock
☐ Blue (negative)	☐ Transmissive type	☐ 3 O' clock
☐ FSTN positive	☐ Others	☐ 9 O' clock
☐ FSTN negative		

LCD MODULE NUMBER NOTATION:

CV320240F- MY - S F - N 6 – T
(1) (2)(3) (4) (5) (6) (7) (8)

*(1)---Model number of standard LCD Modules
*(2)---Backlight type
N – No backlight
E – EL backlight
L – Side-lited LED backlight
M– Array LED backlight
C – CCFL
*(3)---Backlight color
N – No backlight
A – Amber
B – Blue
O– Orange
W–White
Y – Yellow green
*(4)---Display mode
T – TN
V – TN (Negative)
S – STN Yellow green
G – STN Grey
B – STN Blue (Negative)
F – FSTN
N – FSTN (Negative)
*(5)---Rear polarizer type
R – Reflective
F – Transflective
T – Transmissive
*(6)---Temperature range
N – Normal
W– Extended
*(7)---Viewing direction
6 – 6 O'clock
2 – 12 O'clock
3 – 3 O'clock
9 – 9 O'clock
*(8)---Special code for other requirements
(Can be omitted if not used)
T – Touch panel (Analog)
P – Touch panel (Digital)

GENERAL DESCRIPTION

Display mode : 320 x 240 dots, graphic LCD module

Interface : 8-bit parallel

Driving method : 1/240 duty, 1/15 bias

Controller IC : RAIO RA8806 or equivalent
For the detailed information, please refer to the IC specifications.

MECHANICAL DIMENSIONS

Item	Dimension	Unit	Item	Dimension	Unit
Outline Dimension			Viewing Area	122.0 (L)x92.0(W)	mm
Non Backlight (N)	161.0(L)x112.0(W)x10.0MAX. (H)	mm	Dot Pitch	0.36(L)x0.36(W)	mm
LED Sided Backlight(L)	161.0(L)x112.0(W)x13.0MAX. (H)	mm	Dot Size	0.33(L)x0.33(W)	mm

CONNECTOR PIN ASSIGNMENT

(CN4)

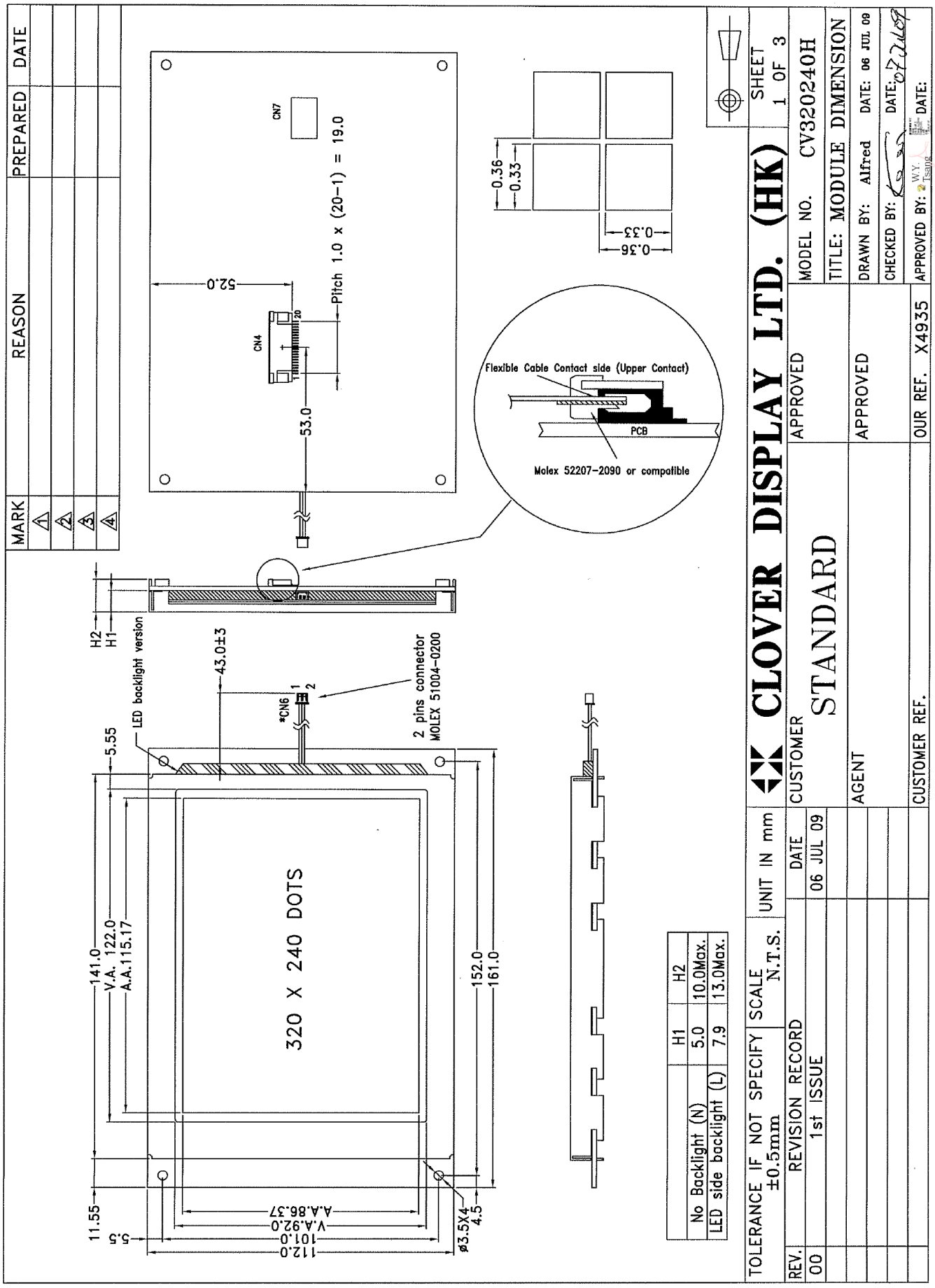
Pin No.	Symbol	Function
1	RS	Register select
2	WR	Write signal
3	RD	Read signal
4	CS1	Chip select 1
5	V0	LCD contrast adjustment
6	VDD	Supply voltage for logic
7	VSS	Ground
8	VEE	Supply voltage for LCD
9	DB0	Data bus
10	DB1	
11	DB2	
12	DB3	
13	DB4	
14	DB5	
15	DB6	
16	DB7	
17	CS2	Chip select 2
18	BSY	Busy signal
19	INT	Interrupt signal
20	RST	Reset signal

(*CN6)

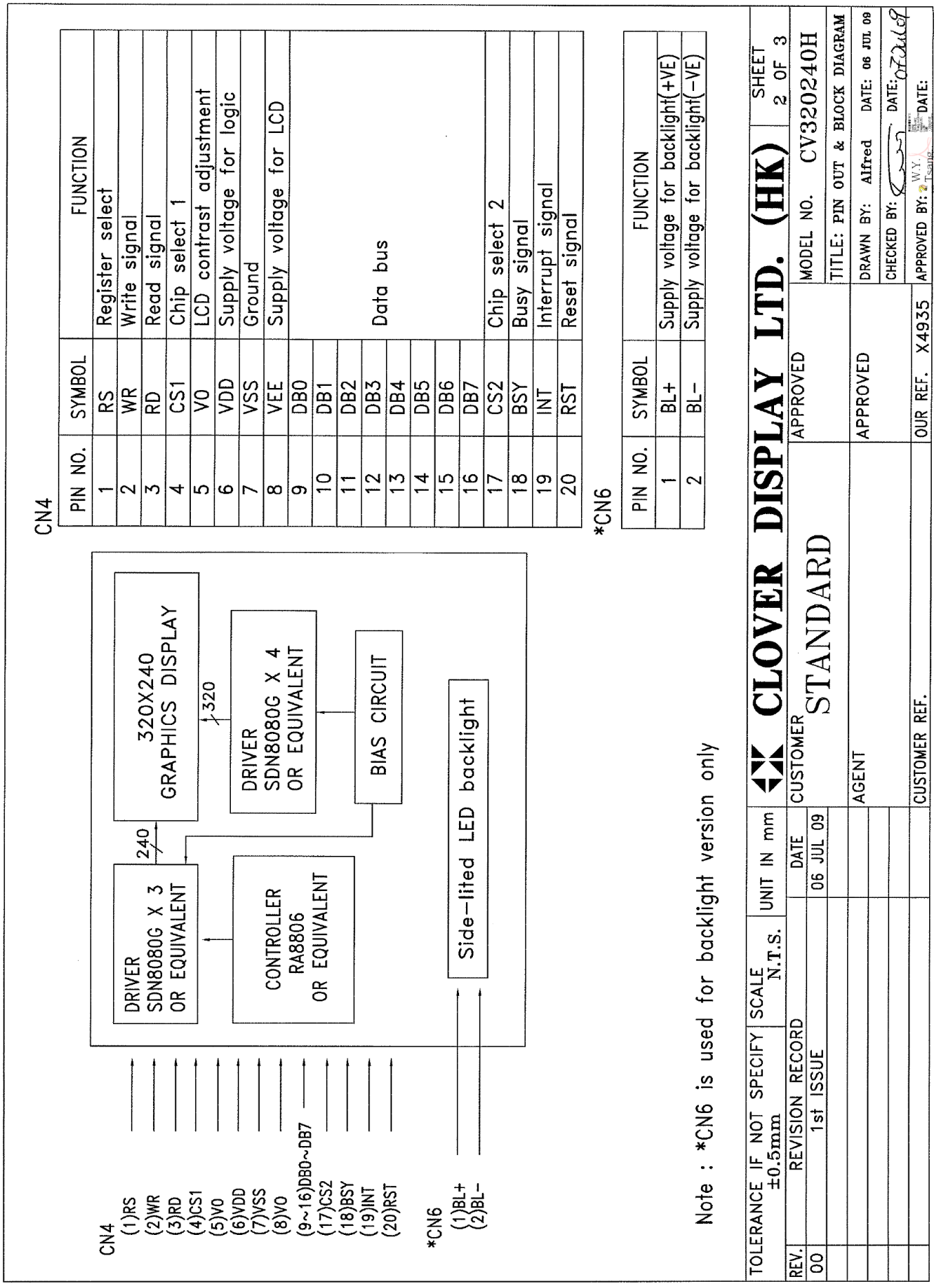
Pin No.	Symbol	Function
1	BL+	Supply voltage for backlight (+VE)
2	BL-	Supply voltage for backlight (-VE)

Note: *CN6 is use for backlight version only

COUNTER DRAWING OF MODULE DIMENSION



COUNTER DRAWING OF PIN OUT & BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS

Conditions: VSS=0V, Ta=25℃

Item	Symbol	MIN.	TYP.	MAX.	Unit	Item	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage for Logic	VDD	4.75	5.0	5.25	V	Input Voltage for LCD	VEE	-20.0	—	-23.0	V
Supply Current for Logic	IDD	—	6	18	mA	"H"Level Input Voltage	VIH	0.8VDD	—	VDD	V
Contrast adjustment for LCD	V0	-18.8	-19.0	-19.2	V	"L"Level Input Voltage	VIL	VSS	—	0.2VDD	V
EL Backlight Voltage (VEL)											
EL(@ Frequency 400Hz)	VBL	—	—	—	Vrms	—	—	—	—	—	—
Side-lited LED Backlight Forward Voltage (VF)(#)						**Side-lited LED Backlight Forward Current (IF)(#)**					
White	VBL	—	3.5	3.8	V	White	IBL	—	120	132	mA
Blue	VBL	—	—	—	V	Blue	IBL	—	—	—	mA
Yellow Green	VBL	—	—	—	V	Yellow Green	IBL	—	—	—	mA

Note (#) : To meet the optimum brightness, the backlight should be driven by constant voltage 3.5V.

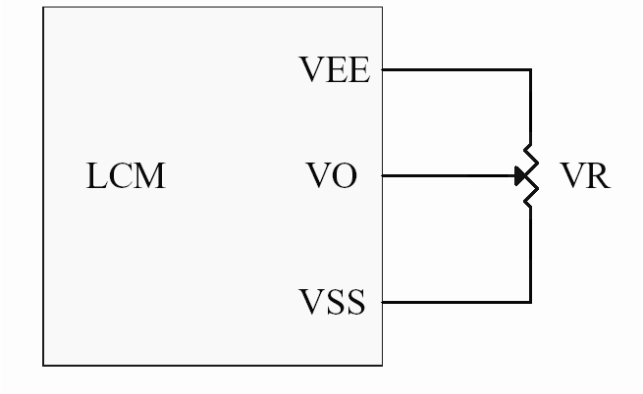
ABSOLUTE MAXIMUM RATINGS

Please make sure not to exceed the following maximum rating values under the worst application conditions.

Item	Symbol	Rating (for normal temperature)	Rating (for wide temperature)	Unit
Supply Voltage for Logic	VDD	-0.3 to 6.5	-0.3 to 6.5	V
Input Voltage for Logic	VIN	-0.3 to VDD+0.3	-0.3 to VDD+0.3	V
Operating Temperature	Topr	0 to 50	-20 to 70	℃
Storage Temperature	Tstg	-10 to 60	-30 to 80	℃

APPLICATION EXAMPLE

A variable resistor is used to adjusting the contrast of the LCD.



Recommend : VR > 50KΩ .

REGISTER LIST TABLE

REG#	Name	D7	D6	D5	D4	D3	D2	D1	D0	Default
--	**STATUS**	MBUSY	SBUSY	SLEEP			WAKE_STS	KS_STS	TP_STS	--
00h	**WLCR**	PWR	LINEAR	SRST	--	TEXT_MD	ZDOFF	GBLK	GINV	00h
01h	**MISC**	NO_ FLICKER	CLKO_SEL	BUSY_ LEV	INT_LEV	XCK_SEL1	XCK_SEL0	SDIR	CDIR	04h
03h	**ADSR**	SCR_PEND	--	--	--	BIT_INV	SCR_DIR	SCR_HV	SCR_EN	00h
0Fh	**INTR**	--	WAKI_EN	KEYI_EN	TPI_EN	TP_ACT	WAK_STS	KEY_STS	TP_STS	00h
10h	**WCCR**	CUR_INC	FULL_OFS	BIT_REV	BOLD	T90DEG	CUR_EN	CUR_BLK	---	00h
11h	**CHWI**	CURH3	CURH2	CURH1	CURH0	ROWH3	ROWH 2	ROWH 1	ROWH 0	00h
12h	**MAMR**	CUR_HV	DISPMD2	DISPMD1	DISPMD0	L_MIX1	L_MIX 0	MW_MD1	MW_MD0	11h
20h	**AWRR**	--	--	AWR5	AWR4	AWR3	AWR2	AWR1	AWR0	27h
21h	**DWWR**	--	--	DWW5	DWW 4	DWW 3	DWW 2	DWW 1	DWW 0	27h
30h	**AWBR**	AWB7	AWB6	AWB5	AWB4	AWB3	AWB2	AWB1	AWB0	EFh
31h	**DWHR**	DWH7	DWH6	DWH5	DWH4	DWH3	DWH2	DWH1	DWH0	EFh
40h	**AWLR**	--	--	AWL5	AWL4	AWL3	AWL2	AWL1	AWL0	00h
50h	**AWTR**	AWT7	AWT6	AWT5	AWT4	AWT3	AWT2	AWT1	AWT0	00h
60h	**CURX**	--	--	CURX5	CURX4	CURX3	CURX2	CURX1	CURX0	00h
61h	**BGSG**	--	--	BGSG5	BGSG4	BGSG3	BGSG2	BGSG1	BGSG0	00h
62h	**EDSG**	EDSG7	EDSG6	EDSG5	EDSG4	EDSG3	EDSG2	EDSG1	EDSG0	00h
70h	**CURY**	CURY7	CURY6	CURY5	CURY4	CURY3	CURY2	CURY1	CURY0	00h
71h	**BGCM**	BGCM7	BGCM6	BGCM5	BGCM4	BGCM3	BGCM2	BGCM1	BGCM0	00h
72h	**EDCM**	EDCM7	EDCM6	EDCM5	EDCM4	EDCM3	EDCM2	EDCM1	EDCM0	00h
80h	**BTMR**	BLKT7	BLKT6	BLKT5	BLKT4	BLKT3	BLKT2	BLKT1	BLKT0	00h
90h	**ITCR**	ITC7	ITC6	ITC5	ITC4	ITC3	ITC2	ITC1	ITC0	00h
A0h	**KSCR1**	KEY_EN	KEY4X8	KSAMP1	KSAMP0	LKEY_EN	KF2	KF1	KF0	00h
A1h	**KSCR2**	KWAK_EN	--	--	--	LKEY_T1	LKEY_T0	KEYNO1	KEYNO0	00h
A2h	**KSDR0**	KSD07	KSD06	KSD05	KSD04	KSD03	KSD02	KSD01	KSD00	00h
A3h	**KSDR1**	KSD17	KSD16	KSD15	KSD14	KSD13	KSD12	KSD11	KSD10	00h
A4h	**KSDR2**	KSD27	KSD26	KSD25	KSD24	KSD23	KSD22	KSD21	KSD20	00h
B0h	**MWCR**	MWD7	MWD6	MWD5	MWD4	MWD3	MWD2	MWD1	MWD0	--
B1h	**MRCR**	MRD7	MRD6	MRD5	MRD4	MRD3	MRD2	MRD1	MRD0	--
C0h	**TPCR1**	TP_EN	TP_SMP2	TP_SMP1	TP_SMP0	TPWAK _EN	ACLK2	ACLK1	ACLK0	00h
C1h	**TPXR**	TPX9	TPX8	TPX7	TPX6	TPX5	TPX4	TPX3	TPX2	00h
C2h	**TPYR**	TPY9	TPY8	TPY7	TPY6	TPY5	TPY4	TPY3	TPY2	00h
C3h	**TPZR**	TPX1	TPX0	--	--	TPY1	TPY0	--	--	00h
C4h	**TPCR2**	MTP_MD	--	--	--	--	--	MTP_PH1	MTP_PH2	00h
D0h	**PCR**	PWM_EN	PWM_DIS_ LEV	--	--	PCLK_R3	PCLK_R2	PCLK_R1	PCLK_R0	00h
D1h	**PDCR**	PDUTY7	PDUTY6	PDUTY5	PDUTY4	PDUTY3	PDUTY2	PDUTY1	PDUTY0	00h
E0h	**PNTR**	PND7	PND6	PND5	PND4	PND3	PND2	PND1	PND0	00h
F0h	**FNCR**	ISO8859_E N	--	--	--	MCLR	ASC	ASC_SEL1	ASC_SEL0	00h
F1h	**FVHT**	FH1	FH0	FV1	FV0	--	--	--	--	00h

REGISTER DESCRIPTION

STATUS Register (RS = 1, ZWR = 1)

Bit	Description	Access
7	**Memory Write Busy Flag** 0 : Not busy. 1 : Busy, when font write or memory clear cycle is running, the busy flag = 1.	R
6	**SCAN_BUSY** 0 : Not busy. 1 : When driver scan logic is not idle(i.e. XCK is active), SCAN_BUSY = 1.	R
5	**SLEEP** 0 : Normal mode. 1 : Sleep mode.	R
4-3	**NA**	R
2	**Wakeup Status bit** (The same with REG[0Fh] Bit-2.)	R
1	**KS Status bit** (The same with REG[0Fh] Bit-1.)	R
0	**TP Status bit** (The same with REG[0Fh] Bit-0.)	R

2	**Set Display On/Off Selection** The bit is used to control LCD Driver Interface signal – "DISP_OFF". 0 : DISP_OFF pin output low(Display Off). 1 : DISP_OFF pin output high(Display On).	0	R/W
1	**Blink Mode Selection** 0 : Normal Display. 1 : Blink Full Screen. The blink time is set by register BTMR.	0	R/W
0	**Inverse Mode Selection** 0 : Normal Display. 1 : Inverse Full Screen. It will cause the display inversed.	0	R/W

REG [01h] Misc. Register (**MISC**)

Bit	Description	Default	Access
7	**Eliminating Flicker** 1 : Eliminating flicker mode, scan will auto-pending when busy. 0 : Normal mode.	0	R/W
6	**Clock Output** (Pin CLK_OUT) Control 1 : The pin "CLK_OUT" indicates the SLEEP state of Status Register(0: Normal Mode, 1: Sleep Mode). 0 : The pin "CLK_OUT" is the output of Internal system clock.	0	R/W
5	**Busy Polarity (for "BUSY" pin)** 1 : Set Active High. 0 : Set Active Low.	0	R/W
4	**Interrupt Polarity (for "INT" pin)** 1 : Set Active High. 0 : Set Active Low.	0	R/W
3-2	**Driver Clock Selection** These two bits are used to select the clock frequency of XCK. 0 0 : XCK = CLK/8 0 1 : XCK = CLK/4 (Default) 1 0 : XCK = CLK/2 1 1 : XCK = CLK The "CLK" means system clock.	01	R/W
1	**SEG Scan Direction**(SDIR) 0 : SEG order is 0 ~ 319. 1 : SEG order is 319 ~ 0.	0	R/W
0	**COM Scan Direction**(CDIR) 0 : COM order 0 ~ 239. 1 : COM order 239 ~ 0.	0	R/W

REG [03h] Advance Display Setup Register (**ADSR**)

Bit	Description	Default	Access
7	**Scroll Function Pending** 1 : Scroll function pending 0 : Scroll function keep active **Note:** When SCR_HV(Bit-1) and SCR_EN(Bit-0) are changed, the function does not support.	0	R/W

6-4	**Reserved**	000	R
3	**BIT_ORDER**(Set driver data output bit order) 1 : Inverse driver output data order(Bit-7 to Bit-0, Bit-6 to Bit-1 and so on) 0 : Normal Mode	0	R/W
2	**SCR_DIR**(Scroll Direction) When SCR_HV = 0(Horizontal Scroll) 0 : Left → Right. 1 : Right → Left. When SCR_HV = 1(Vertical Scroll) 0 : Top → Bottom. 1 : Bottom → Top.	0	R/W
1	**SCR_HV**(Scroll Horizontal/Vertical) 0 : Segment Scrolling(Horizontal). 1 : Common Scrolling(Vertical).	0	R/W
0	**SCR_EN**(Scroll Enable) 1 : Scroll function enable. 0 : Scroll function disable.	0	R/W

REG [0Fh] Interrupt Setup and Status Register (**INTR**)

Bit	Description	Default	Access
7	**Reserved**	0	R
6	**Wakeup Interrupt Mask** 1 : Enable wake-up Interrupt. 0 : Disable wake-up Interrupt.	0	R/W
5	**Key-Scan Interrupt Mask** 1 : Enable Key-Scan Interrupt. 0 : Disable Key-Scan Interrupt.	0	R/W
4	**Touch Panel Interrupt Mask** 1 : Generate interrupt output if touch panel was detected. 0 : Don't generate interrupt output if touch panel was detected.	0	R/W
3	**Touch Panel Event**(Only activate in TP Manual mode) 1 : Touch panel is touched. 0 : Touch panel is not touched.	0	R
2	**Wakeup Interrupt Status bit** 1 : Interrupt that indicate wake-up event happen from Sleep mode. 0 : No wake-up interrupt happen. User must write "0" to clear the Status bit.	0	R/W
1	**Key-Scan Interrupt Status bit** 1 : Key-Scan Detects Key Input. 0 : Key-Scan doesn't Detect Key Input. User must write "0" to clear the Status bit.	0	R/W
0	**Touch Panel Detect Status bit** 1 : Touch Panel Touched. 0 : Touch Panel Untouched. User must write "0" to clear the Status bit.	0	R/W

REG [10h] Whole Chip Cursor Control Register (**WCCR**)

Bit	Description	Default	Access
7	**CUR_INC** (Auto Increase Cursor Position in Reading/Writing DDRAM Operation.) 1 : Disable. 0 : Enable(Auto Increase).	0	R/W
6	**FULL_OFS (Full-size and Half-size Character Alignment)** 1 : Enable, in Full-size and Half-size character mixed mode. Chinese always start at full-size alignment. 0 : Disable.	0	R/W
5	**Reversed Data Write mode** 0 : Store Current Data to DDRAM Directly. 1 : Store Current Data to DDRAM Inversely.(i.e. 01101101➔ 10010010)	0	R/W
4	**Bold Font (Character Mode Only)** 1 : Bold Font 0 : Normal Font	0	R/W
3	**Font Rotate mode(T90DEG)** 1 : Font rotates 90 degree. (See Section 6-10-4 for detail) 0 : Normal font.	0	R/W
2	**Cursor Display** 1 : Set Cursor Display On. 0 : Set Cursor Display Off.	0	R/W
1	**Cursor Blinking** 1 : Blink Cursor. The blink time is determined by register BTMR. 0 : Normal.	0	R/W
0	**Reserved**	0	R

REG [11h] Cursor Height and Word Interval Register (**CHWI**)

Bit	Description	Default	Access
7-4	**Set Cursor Height** 0000 b → Height = 1 pixel. 0001 b → Height = 2 pixels. 0010 b → Height = 3 pixels. : : 1111 b → Height = 16 pixels. **Note:** In normal font, the cursor width fixed to one byte(8 pixels). And cursor's height is from 1~16pixels that depends on Bit[7:4]. In vertical font, the cursor height fixed to 16 pixels, and width is from 1~8 pixels that depends on Bit[6:4].	0000	R/W
3-0	**Set Line Gap** 0000 b → Gap = 1 pixel. 0001 b → Gap = 2 pixels. 0010 b → Gap = 3 pixels. : : 1111 b → Gap = 16 pixels.	0000	R/W

REG [12h] Memory Access Mode Register (**MAMR**)

Bit	Description	Default	Access
7	**Cursor Auto Shifting Direction** 0 : Cursor moves horizontally (left to right) first then vertically (top to down). 1 : Cursor moves vertically first then horizontally. **Note:** In graphic mode, the cursor moving is treated as unit of bytes in horizontal direction. At vertical direction, it's treated as unit of bit. At text mode, the bit is ignored, and the cursor moving is always in horizontal direction.	0	R/W
6-4	**Display Layer and Display Mode Selection** 0 0 0 : Gray Mode. In this mode, each pixel consists with 2 continuous bits in memory data. With the FRC methodology, 4-level-gray mode is implemented. The bit mapping is list as below. bit1 bit0 Gray 0 0 Level1 (Lightest) 0 1 Level2 1 0 Level3 1 1 Level4 (Darkest) **Note:** Gray mode doesn't support text-mode input. 0 0 1 : Show DDRAM1 data on screen. 0 1 0 : Show DRRAM2 data on screen. 0 1 1 : Show Two Layer Mode. The display rule depends on Bit-3 and Bit-2 as following. 1 0 X : NA. 1 1 0 : Extension Mode (1), the panel will show both DDRAM1 and DDRAM2 data on the screen. The RA8806 is available for 640x240 pixels panel. 1 1 1 : Extension Mode (2), the panel will show both DDRAM1 and DDRAM2 on the screen. The RA8806 is available for 320x480 pixels panel.	001	R/W
3-2	**Two Layer Mode Selection** Combine the data of DDRAM1 and DDRAM2 on the screen when Bit[6:4] is set as "011". 0 0 : DDRAM1 "OR" DDRAM2. 0 1 : DDRAM1 "XOR" DDRAM2. 1 0 : DDRAM1 "NOR" DDRAM2. 1 1 : DDRAM1 "AND" DDRAM2.	00	R/W
1-0	**MPU Read/Write Layer Selection** 0 0 : Access CGRAM.(512Byte) 0 1 : Access DDRAM1. 1 0 : Access DDRAM2. 1 1 : Access both DDRAM1 and DDRAM2 concurrently	01	R/W

REG [20h] Active Window Right Register (**AWRR**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Active Window Right Position → Segment-Right** **Note:** AWRR must be equal or larger then AWLR, and less or equal then the value 27h (40 in decimal).	27h	R/W

Note:

REG[20h, 30h, 40h, and 50h] are used to dominate an active window for line/row changing when writing data. Users can use these four registers to set the left/right/top/bottom boundary of active window. When data goes beyond the right boundary of it, the cursor will automatically change the next line to write data. It will move to the left boundary of new line in active window. When the data comes to the right-bottom corner, the next write will cause the cursor to move to the left-top corner.

REG [21h] Display Window Width Register (**DWWR**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Set Display Window Width Position → Segment-Width** **Segment-Right = (Segment Number / 8) – 1** If LCD panel resolution is 320x240, the value of the register is: (320 / 8) - 1 = 39 = 27h	27h	R/W

Note:

REG[21h, 31h] are used to set Display Window Resolution. Users can set the viewing scope of Display Data RAM. Column width (DWWR) of RA8806 can be set between 0h ~ 27h, and Row height (DWHR) can be set between 0h ~ EFh.

REG [30h] Active Window Bottom Register (**AWBR**)

Bit	Description	Default	Access
7-0	**Active Window Bottom Position → Common-Bottom** **Note:** AWBR must be equal or larger then AWTR, and less or equal then the value EFh(239 in decimal)	EFh	R/W

REG [31h] Display Window Height Register (**DWHR**)

Bit	Description	Default	Access
7-0	**Display Window Height Position → Common- Height** **Common_ Height = LCD Common Number –1** If LCD panel resolution is 320x240, the value of the register is: 240 – 1 = 239 = EFh	EFh	R/W

REG [40h] Active Window Left Register (**AWLR**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Active Window Left Position → Segment-Left** **Note:** AWLR must be equal or less then AWRR, and less then the value 27h(39 in decimal)	00h	R/W

REG [50h] Active Window Top Register (**AWTR**)

Bit	Description	Default	Access
7-0	**Active Window Top Position → Common-Top** **Note:** AWTR must be equal or less then AWBR, and less then the value EFh (239 in decimal)	00h	R/W

REG [60h] Cursor Position X Register (**CURX**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Cursor Position of Segment / RAM0 Address[4:0]** Define the cursor address of segment, a value from 0h ~ 27h(0 ~ 40 in decimal) When CGRAM write mode is selected (REG[12h] Bit[1:0] = 00b), the Bit[4:0] is the address for writing bit-map data. When create a full-size font, normally set to 0. When create an odd half-size font, normally set to 0, and set 10h for even font.	00h	R/W

REG [61h] Begin Segment Position Register of Scrolling (**BGSG**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Segment Start Position of Scrolling Mode** REG[61h] defines the start position (left boundary) of scroll window, it must be a value that less or equal to the REG[62h], which defines the end position(right boundary) of scroll window. Also it must be less then the value of 27h (40 in decimal), for the Display Data RAM limit.	00h	R/W

Note:

REG[61h, 62h, 71h, 72h] dominate a named scroll window for scroll function. They must be set before the scroll function is enable.

REG [62h] End Segment Position Register of Scrolling (**EDSG**)

Bit	Description	Default	Access
7-6	**Reserved**	00	R
5-0	**Segment End Position of Scrolling Mode** REG[62h] defines the end position(right boundary) of scroll window, it must be a value that larger or equal to the REG[61h], which defines the end position(left boundary) of scroll window. Also it must be less or equal then the value of 27h(40 in decimal), for the Display Data RAM limit.	00h	R/W

REG [70h] Cursor Position Y Register (**CURY**)

Bit	Description	Default	Access
7-0	**Cursor Position of Common / RAM0 Address[8:5]** Define the cursor address of common, a value from 0h ~ EFh(0 ~ 239 in decimal). When CGRAM write mode is selected (REG[12h] Bit[1:0] = 00b), the Bit[3:0] is indicate which font will be created. And Bit[7:4] are not available.	00h	R/W

REG [71h] Scrolling Action Range Begin Common Register (**BGCM**)

Bit	Description	Default	Access
7-0	**Common Start Position of Scrolling Mode** REG[71h] defines the begin position(top boundary) of scroll window, it must be a value that less or equal to the REG[72h], which defines the end position(bottom boundary) of scroll window. Also it must be less then the value of EFh (239 in decimal), for the Display Data RAM limit.	00h	R/W

REG [72h] Scrolling Action Range END Common Register (**EDCM**)

Bit	Description	Default	Access
7-0	**Common Ending Position of Scrolling Mode** REG[72h] defines the end position(bottom boundary) of scroll window, it must be a value that larger or equal to the REG[71h], which defines the end position(top boundary) of scroll window. Also it must be less or equal then the value of EFh (239 in decimal), for the Display Data RAM limit.	00h	R/W

REG [80h] Blink Time Register (**BTMR**)

Bit	Description	Default	Access
7-0	**Cursor Blink Time and Scroll Time** **Blinking Time = Bit[7:0] x (Frame width)** **Frame width = 1/Frame Rate** The Frame Rate is depends on the DWWR and DWHR and ITCR setting.	00h	R/W

Notes:

1. The Setting also determines the scroll moving speed.
2. The Frame width is the time that the controller scan whole panel, it depends on the system clock frequency, setting of display window, driver interface (4-bits/8-bits), Idle time (ITCR), and dual mode or gray scale mode, etc.

REG [90h] Idle Time Counter Register (**ITCR**)

Bit	Description	Default	Access
7-0	**Idle Time Setting, in count of system clock.** The value can determine the scan time of each COM of the LCD. **COM_PRD = (COM_SCAN + ITCR) x XCK_PRD** In which, **COM_SCAN = (SEG_NO/LD_WIDTH) x (1 + EXT_MD)** **XCK_PRD = 1 / XCK** **COM_PRD:** The finally scan period for each COM(Unit : ns). **COM_SCAN:** The really scan time for each COM. **XCK_PRD:** One cycle time of XCK. XCK is depends on the system clock(CLK) and REG[01h] Bit[3:2]. If system clock is 8MHz, REG[01h] Bit[3:2] = 10b, then XCK_PRD = 250ns. **SEG_NO:** Segment number, i.e. 240x160 panel, SEG_NO = 240. **EXT_MD:** In extension mode1 or 2(REG[12h] Bit[6:4] = 111b or 110b), the EXT_MD = 1, otherwise EXT_MD = 0. **LD_WIDTH:** Driver data width. If LCD driver data bus is 4-bits then LD_WIDTH = 4. If LCD driver data bus is 8-bits then LD_WIDTH = 8. Please refer pin "DW" description of Section 4-3.	00h	R/W

REG [A0h] Key-Scan Control Register 1 (**KSCR1**)

Bit	Description	Default	Access
7	**Key-Scan Enable Bit** 1 : Enable. 0 : Disable.	0	R/W
6	**Key-Scan Matrix Selection** 1 : 4x8 Matrix(KOUT[3:0] is used, KOUT[7:4] please keep floating) 0 : 8x8 Matrix(KOUT[7:0] is used)	0	R/W
5-4	**Key-Scan Data Sampling Times** De-bounce times of scan frequency. 0 0 : 4 0 1 : 8 1 0 : 16 1 1 : 32	00	R/W
3	**LNGKEY_EN : Long Time Key Function Enable** LNGKEY_EN = 0 → Long key function is disable. LNGKEY_EN = 1 → Long key function is enable.	0	R/W

<table>
<tr>
<td>2-0</td>
<td>KF2-0: Key-Scan frequency.
If system clock is 10MHz, then the related Key-Scan timing are as following:
<table>
<tr><th>KF2</th><th>KF1</th><th>KF0</th><th>Key-Scan Pulse Width (KOUT period)</th><th>Key-Scan Cycle (4x8)</th><th>Key-Scan Cycle (8x8)</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>16µs</td><td>64µs</td><td>128µs</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>32µs</td><td>128µs</td><td>256µs</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>64µs</td><td>256µs</td><td>512µs</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>128µs</td><td>512µs</td><td>1.024ms</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>256µs</td><td>1.024ms</td><td>2.048ms</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>512µs</td><td>2.048ms</td><td>4.096ms</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>1.024ms</td><td>4.096ms</td><td>8.192ms</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>2.048ms</td><td>8.192ms</td><td>16.384ms</td></tr>
</table>
</td>
<td>000</td>
<td>R/W</td>
</tr>
</table>

REG [A1h] Key-Scan Controller Register 2(**KSCR2**)

Bit	Description	Default	Access
7	**Key-Scan Wakeup Function Enable Bit** 0: Key-Scan Wakeup function is disable. 1: KEY-SCAN Wakeup function is enable.	0	R/W
6-4	**Reserved**	000	R
3-2	**Long Key Timing Adjustment** 00 : About 0.625sec(for 8MHz Clock source) 01 : About 1.25sec(for 8MHz Clock source) 10 : About 1.875 sec(for 8MHz Clock source) 11 : About 2.5 sec(for 8MHz Clock source)	00	R/W
1-0	**Numbers of Key Hit.** 00 : No key is pressed 01 : One key is pressed, read REG[A2h] for the key number. 10 : Two key is pressed, read REG[A2h ~ A3h] for the key number. 11 : Three key is pressed, read REG[A2h ~ A4h] for the key number.	00	R

REG [A2h ~ A4h] Key-Scan Data Register (**KSDR0 ~ 2**)

Bit	Description	Default	Access
7-0	**Key Strobe Data** The corresponding key number that is pressed. Please reference Section 6-5 "Key-Scan".	00h	R

REG [B0h] Memory Write Command Register (**MWCR**)

Bit	Description	Default	Access
7-0	**Memory data write command from the cursor position.** **Note:** Write memory data, user must write the MWCR command first, then write DATA cycle.	NA	R/W

REG [B1h] Memory Read Command Register (**MRCR**)

Bit	Description	Default	Access
7-0	**Memory data read command from the cursor position.** **Note:** Memory read cycle in text mode, the cursor move in same behavior like graphic mode. B1h will perform a pre-read function. So the cursor position will increase after the MRCR command is write.	NA	R/W

REG [C0h] Touch Panel Control Register 1 (**TPCR1**)

Bit	Description	Default	Access
7	**Touch Panel Enable Bit** 1 : Enable. 0 : Disable.	0	R/W
6-4	**TP Sample Time Adjusting** 000 : Wait 50μs for ADC data ready. 001 : Wait 100μs for ADC data ready. 010 : Wait 200μs for ADC data ready. 011 : Wait 400μs for ADC data ready. 100 : Wait 800μs for ADC data ready. 101 : Wait 1.6ms for ADC data ready. 110 : Wait 3.2ms for ADC data ready. 111 : Wait 6.4ms for ADC data ready. **Note:** When touch panel detects the Touch event, to avoid the signal instability, the sampled time is delayed to wait the signal stable. The TP Sample Time Adjusting and ADC Clock Convert Speed relation just refer to Section 6-4-3.	000	R/W
3	**Touch Panel Wake-up Enable:** 1 : Touch panel can wake-up the Sleep mode(At the condition that ADC is enabled). 0 : Disable the touch panel wake-up function	0	R/W
2-0	**ADC Clock Convert Speed** 0 0 0 : CLK / 4 0 0 1 : CLK / 8 0 1 0 : CLK /16 0 1 1 : CLK / 32 1 0 0 : CLK / 64 1 0 1 : CLK / 128 1 1 0 : CLK / 256 1 1 1 : CLK / 512 The “CLK” means system clock.	000	R/W

REG [C1h] Touch Panel X High Byte Data Register (**TPXR**)

Bit	Description	Default	Access
7-0	**Touch Panel X Data Bit[9:2](Segment)**	00h	R

REG [C2h] Touch Panel Y High Byte Data Register (**TPYR**)

Bit	Description	Default	Access
7-0	**Touch Panel Y Data Bit[9:2] (Common)**	00h	R

REG [C3h] Touch Panel Segment/Common Low Byte Data Register (**TPZR**)

Bit	Description	Default	Access
7-4	**Reserved**	0000	R
3-2	**Touch Panel Y Data Bit[1:0] (Common)**	00	R
1-0	**Touch Panel X Data Bit[1:0] (Segment)**	00	R

REG [C4h] Touch Panel Control Register 2 (**TPCR2**)

Bit	Description	Default	Access
7	**TP Manual Mode Enable** 1 : Using the manual mode. 0 : Auto mode.	0	R/W
6-2	**Reserved**	00h	R
1-0	**Mode selection for TP Manual Mode** 00 : IDLE mode: ADC idles. 01 : Wait for TP event, touch panel event could cause the interrupt or be read from REG[0Fh] B3. 10 : Latch X data, in the phase, X Data can be latched in REG[C1h] and REG[C3h]. 11 : Latch Y data, in the phase, Y Data can be latched in REG[C2h] and REG[C3h].	00	R/W

REG [D0h] PWM Control Register (**PCR**)

Bit	Description	Default	Access
7	**PWM enable** 1 : Enable 0 : Disable, PWM_OUT level depends on the REG[D0h] Bit-6.	0	R/W
6	**PWM Disable Level** 0 : PWM_OUT is Normal L when PWM disable or Sleep mode. 1 : PWM_OUT is Normal H when PWM disable or Sleep mode.	0	R/W
5-4	**Reserved**	00	R
3-0	**PWM Clock Source Divide Ratio** 0000 b → CLK / 1 0001 b → CLK / 2 0010 b → CLK / 4 0011 b → CLK / 8 : : 1111 b → CLK / 32768 The “CLK” means system clock. For example, CLK is 8MHz: 0000 b ➔ PWM clock source = 8MHz, 0001 b ➔ PWM clock source = 4MHz, : : 1111 b ➔ PWM clock source = 256Hz.	0000	R/W

REG [D1h] PWM Duty Cycle Register (**PDCR**)

Bit	Description	Default	Access
7-0	**PWM Cycle Duty Selection Bit** 00h → 1 / 256 01h → 2 / 256 High period 02h → 3 / 256 High period : : FFh → 256 / 256 High period	00h	R/W

REG [E0h] Pattern Data Register (**PNTR**)

Bit	Description	Default	Access
7-0	**Data Written to DDRAM(Display Data RAM)** The pattern that will be filled to active window in memory clear function. When REG[F0h] Bit-3 is '1', the data in the REG[E0h] will be filled to the whole active window.	00h	R/W

REG [F0h] Font Control Register (**FNCR**)

Bit	Description	Default	Access
7	**ISO8859 Mode** 0 : Disable. The contents of ASCII block 1 ~ 4 are show as Table C-1~ Table C-4 of Appendix B. 1 : Enable. The ASCII block 1 ~ 4 indicate the ISO8859-1 ~ 4 standard and show as Table C-5 ~ Table C-8 of Appendix C.	0	R/W
6-4	**Reserved**	000	R
3	**Memory Clear Function** Write Function 0 : No Action. 1 : Memory clear function active, fill the data of FNTR to Active window. When this bit is set to "1", RA8806 will automatically read PNTR data, and fill it to Active window (Range: [AWLR, AWTR] ~ [AWRR, AWBR]), after clear completed, this bit will be cleaned to "0".	0	R/W
2	**ASCII Mode Enable** 1 : All input data will be decoded as ASCII (00h ~ FFh) 0 : In text mode (REG[00h] Bit-3), the RA8806 will check the first written byte data first. If less then 80h then it's treated as ASCII (Half-size). Or it's treated as a full-size text(GB, BIG5 or User-created font).	0	R/W
1-0	**ASCII Blocks Select** 0 0 : Map to ASCII block 1. (Table C-1 and Table C-5 of Appendix C.) 0 1 : Map to ASCII block 2. (Table C-2 and Table C-6 of Appendix C.) 1 0 : Map to ASCII block 3. (Table C-3 and Table C-7 of Appendix C.) 1 1 : Map to ASCII block 4. (Table C-4 and Table C-8 of Appendix C.)	00	R/W

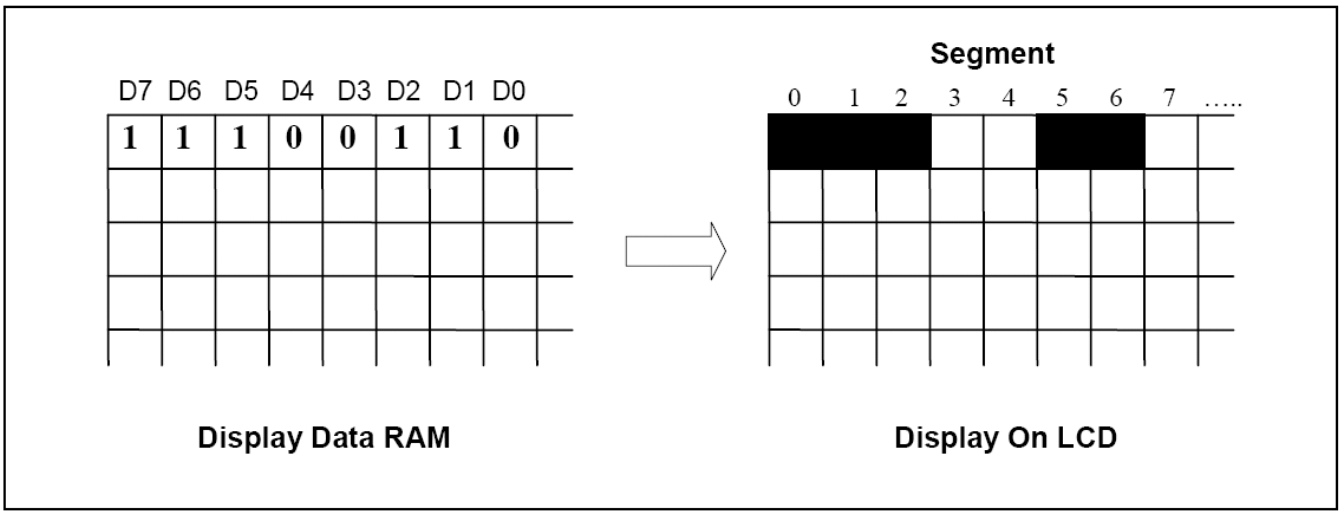
REG [F1h] Font Size Control Register (**FVHT**)

Bit	Description	Default	Access
7-6	**Set Character Horizontal Size** 0 0 : One Time of normal font width. 0 1 : Two Times of normal font width. 1 0 : Three Times of normal font width. 1 1 : Four Times of normal font width.	00	R/W
5-4	**Set Character Vertical Size** 0 0 : One Time of normal font height. 0 1 : Two Times of normal font height. 1 0 : Three Times of normal font height. 1 1 : Four Times of normal font height.	00	R/W
3-0	**Reserved**	0000	R

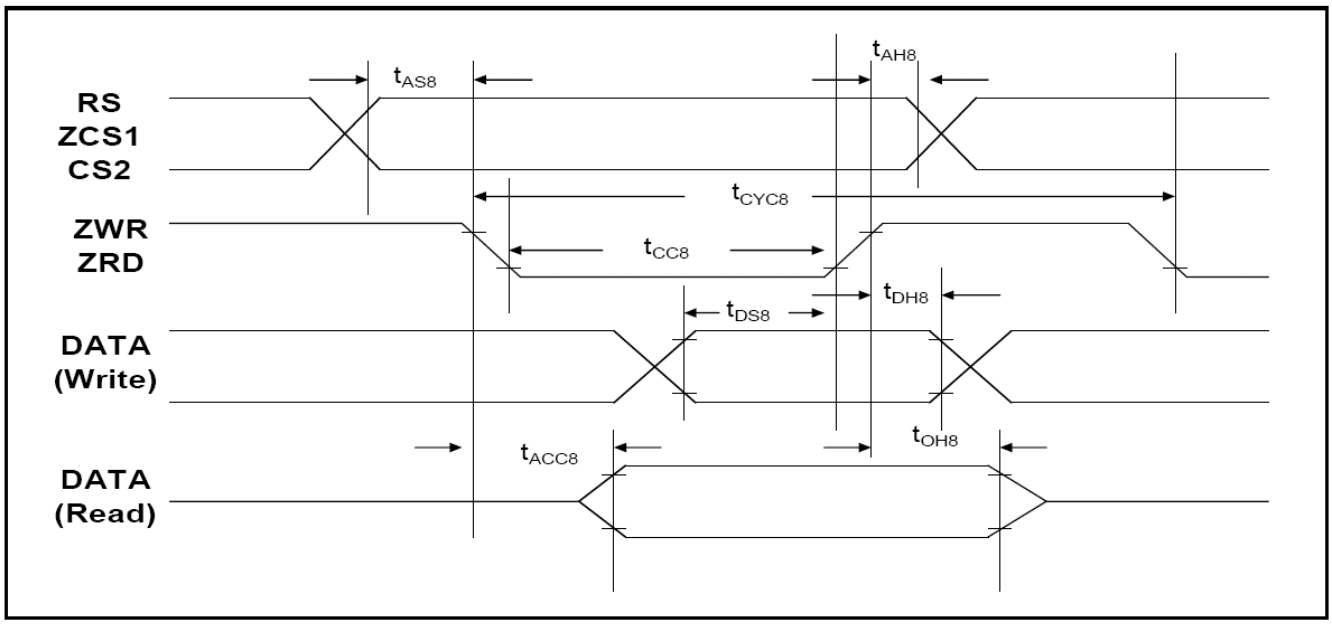
RECOMMENDED INITIAL SETTINGS

Register	Function	Value setting
REG[21H]	Display Window Width Register	27H
REG[31H]	Display Window Height Register	EFH
REG[20H]	Active Window Right Register	27H
REG[30H]	Active Window Bottom Register	EFH
REG[40H]	Active Window Left Register	00H
REG[50H]	Active Window Top Register	00H
REG[00H]	Whole Chip LCD Controller Register	04H
REG[01H]	Misc. Register	A4H
REG[03H]	Advance Display Setup Register	04H
REG[0FH]	Interrupt Setup and Status Register	20H
REG[10 H]	Whole Chip Cursor Control Register	40H
REG[11H]	Cursor Height and Word Interval Register	00H
REG[12 H]	Memory Access Mode Register	11H
REG[60H]	Cursor Position X Register	00H
REG[70H]	Cursor Position Y Register	00H
REG[61H]	Begin Segment Position Register of Scrolling	00H
REG[62H]	End Segment Position Register of Scrolling	00H
REG[71H]	Scrolling Action Range Begin Common Register	00H
REG[72H]	Scrolling Action Range END Common Register	00H
REG[80H]	Blink Time Register	00H
REG[90H]	Idle Time Counter Register	27H
REG[A0H]	Key-Scan Control Register 1	00H
REG[A1H]	Key-Scan Controller Register 2	00H
REG[C0H]	Touch Panel Control Register 1	00H
REG[C4H]	Touch Panel Control Register 2	00H
REG[D0H]	PWM Control Register	00H
REG[D1H]	PWM Duty Cycle Register	00H
REG[E0H]	Pattern Data Register	00H
REG[F0H]	Font Control Register	00H
REG[F1H]	Font Size Control Register	00H

DISPLAY DATA RAM



PARALLEL INTERFACE TIMING DIAGRAM (8080 MODE)

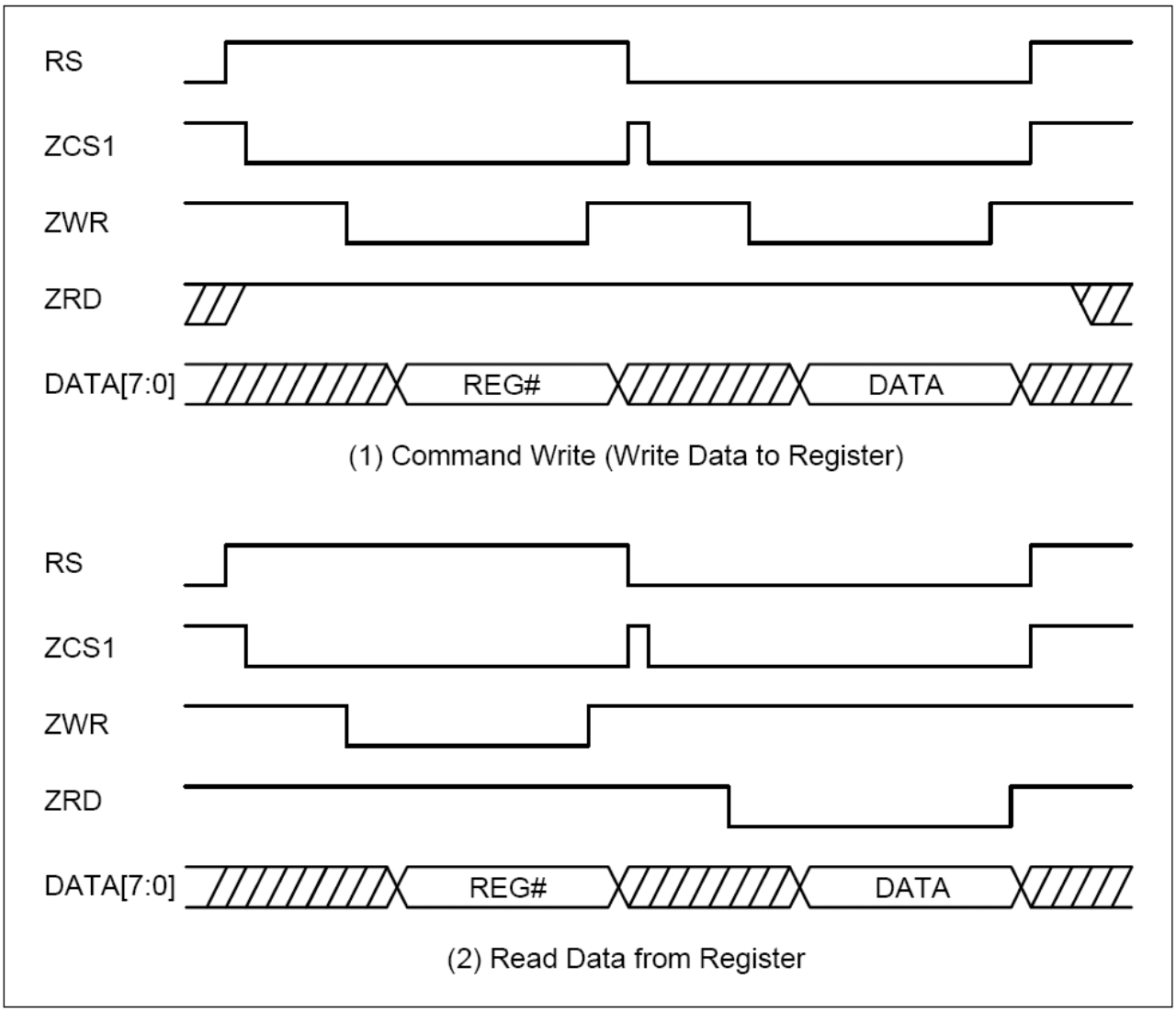


PARALLEL INTERFACE TIMING CHARACTERISTICS (8080 MODE)

Symbol	Description	Rating		Unit	Condition
		Min.	Max.		
t_{CYC8}	Cycle time	2*tc	--	ns	tc = one system clock period
t_{CC8}	Strobe Pulse width	50	--	ns	
t_{AS8}	Address setup time	0	--	ns	
t_{AH8}	Address hold time	20	--	ns	
t_{DS8}	Data setup time	30	--	ns	
t_{DH8}	Data hold time	20	--	ns	
t_{ACC8}	Data output access time	0	20	ns	
t_{OH8}	Data output hold time	0	10	ns	

DATA ACCESS WITH MCU

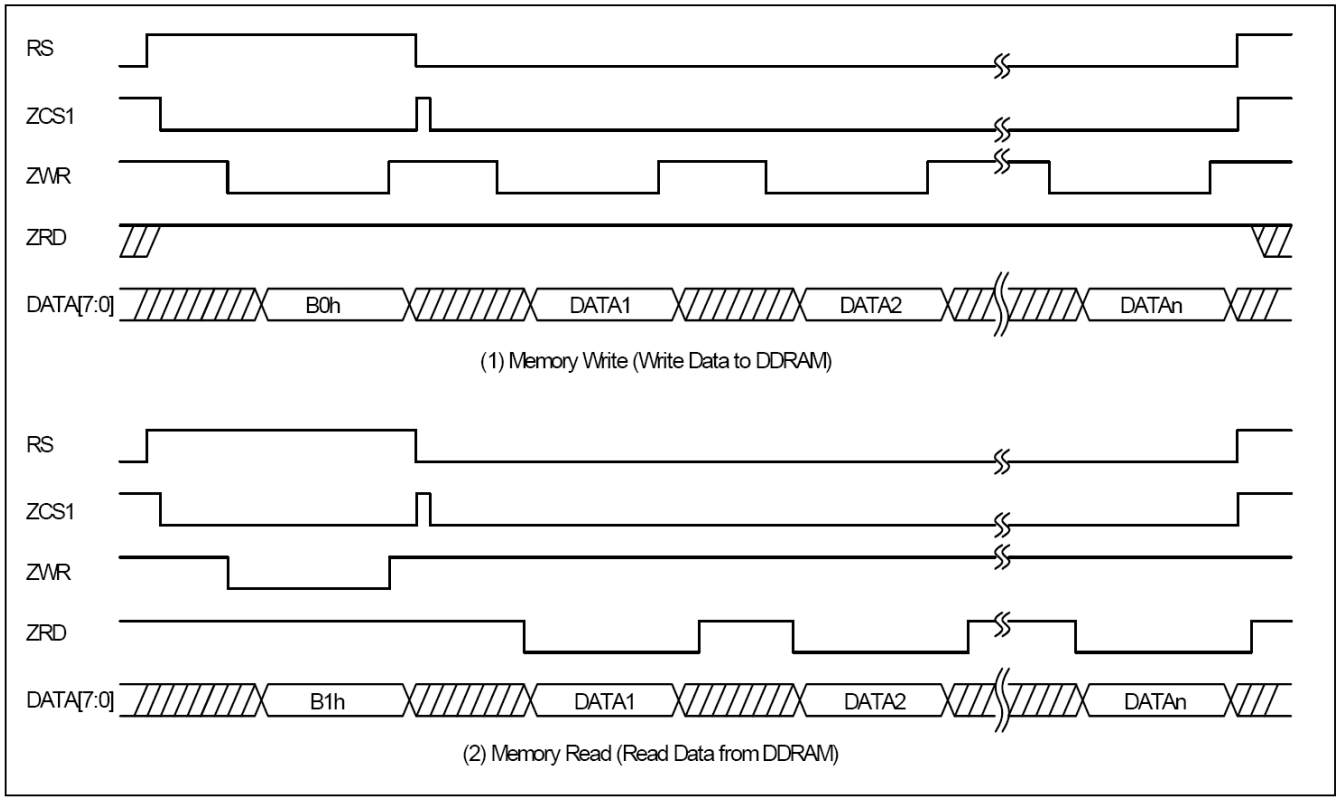
COMMAND WRITE



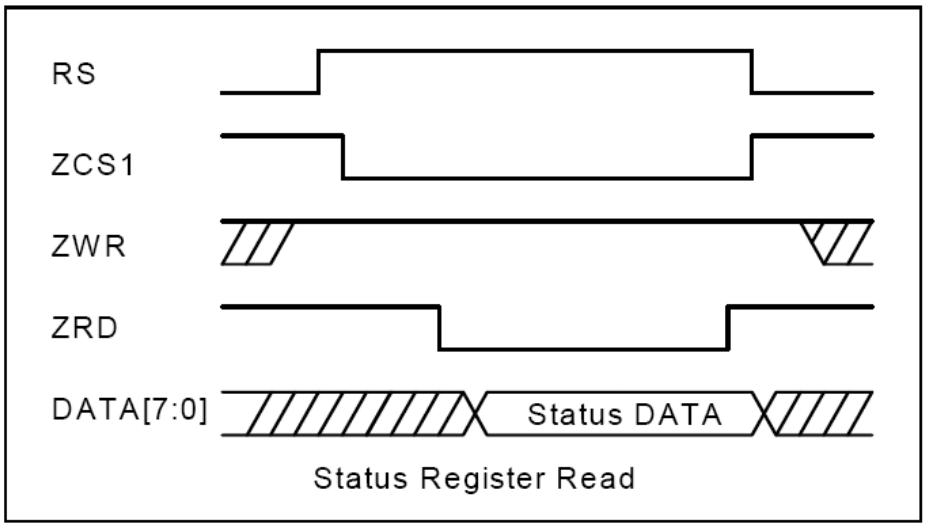
Command Access Time Table

System Clock	Command Access Time
4MHz	1μs
6 MHz	667ns
8 MHz	500ns
10 MHz	400ns
12 MHz	333ns

MEMORY READ/WRITE



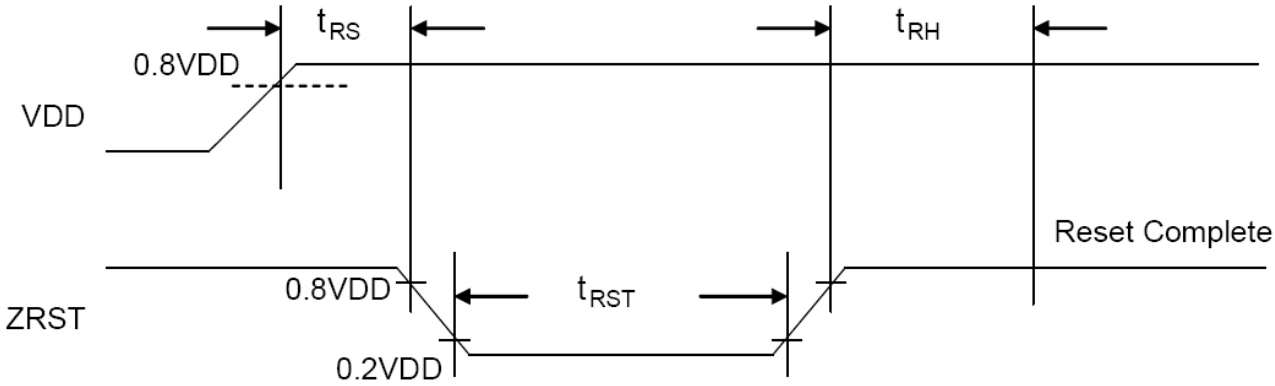
Memory Write/Read Cycle



Status Read Cycle

RESET TIMING DIAGRAM

The RA8806 cannot receive commands while it is reset. Commands to initialize the internal registers should be issued soon after a reset. During reset, the LCD drive signals XD, LP and FR are halted. A delay of 1ms (minimum) is required following the rising edges of both ZRST and VDD to allow for system stabilization. Please refer to Figure 6-28 for more detail description.



RESET TIMING

		Max.	Typ.	Min.	Unit
t_{RS}	Reset setup time	--	--	1	ms
t_{RH}	Reset hold time	--	--	1	ms
t_{RST}	Reset active time	--	--	1024	t_c (*)

*t_C is the period of system clock,
for example: 10MHz, t_C = 100ns

ELECTRO-OPTICAL CHARACTERISTICS

MEASURING CONDITION: POWER SUPPLY = V_{OP} / 64 Hz
TEMPERATURE = 22 ± 5 °C
RELATIVE HUMIDITY = 60 ± 15 %

ITEM	SYMBOL	UNIT	TYP. STN
RESPONSE TIME	Ton	ms	370
	Toff	ms	470
CONTRAST RATIO	Cr	-	7
VIEWING ANGLE (Cr ≥ 2)	$V_{3:00}$	°	40
	$V_{6:00}$	°	50
	$V_{9:00}$	°	40
	$V_{12:00}$	°	30

THE ELECTRO-OPTICAL CHARACTERISTICS ARE MEASURED VALUE BUT NOT GUARANTEED ONES.

RELIABILITY OF LCD MODULE

ITEM	TEST CONDITION FOR NORMAL TEMPERATURE	TEST CONDITION FOR WIDE TEMPERATURE	TIME
High temperature operating	50°C	70°C	240 hours
Low temperature operating	0°C	-20°C	240 hours
High temperature storage	60°C	80°C	240 hours
Low temperature storage	-10°C	-30°C	240 hours
Temperature-humidity storage	40°C 90% R.H.	60°C 90% R.H.	96 hours
Temperature cycling	-10°C to 60°C 30 Min Dwell	-30°C to 80°C 30 Min Dwell	5 cycle
Vibration Test at LCM Level	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	Freq 10-55 Hz Sweep rate: 10-55-10 at 1 min Sweep mode Linear Displacement: 2 mm p-p 1 Hour each for X, Y, Z	—

QUALITY STANDARD OF LCD MODULE

1.0	**Sampling Method**		
	Sampling Plan : MIL STD 105 E Class of AQL : Level II/Single Sampling Critical : 0.25% Major 0.65% Minor 1.5%		
2.0	**Defect Group**	**Failure Category**	**Failure Reasons**
	Critical Defect 0.25%(AQL)	Malfunction	Open Short Burnt or dead component Missing part/improper part P.C.B. Broken
	Major Defect 0.65%(AQL)	Poor Insulation	Potential short High current Component damage or scratched or Lying too close improper coating
		Poor Conduction	Damage joint Wrong polarity Wrong spec. part Uneven/intermittent contact Loose part Copper peeling Rust or corrosion or dirt‘s
	Minor Defect 1.5%(AQL)	Cosmetic Defect	Minor scratch Flux residue Thin solder Poor plating Poor marking Crack solder Poor bending Poor packing Wrong size

HANDLING PRECAUTIONS

(1) CAUTION OF LCD HANDLING & CLEANING

The polarizing plate on the surface of the panel is made from organic substances. Be very careful for chemicals not to touch the plate or it leads the polarizing plate to deteriorate.

If the use of a chemical is unavoidable, wipe the panel lightly with soft materials, such as gauze and absorbent cotton, soaked in a solvent.

*Usable solvent: Alcohol (ethanol, IPA and the like)
*Appropriate solvent: Ketones, ethyl alcohol

Avoid wiping with a dry cloth, since it could damage the surface of the polarizing plate and others.

(2) CAUTION AGAINST STATIC CHARGE

The LCD modules use CMOS LSI drivers, so customers are recommended that any unused input terminal would be connected to V_{DD} or V_{SS}, do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

(3) PACKAGING

Avoid intense shock and falls from a height and do not operate or store them exposed to direct sunshine or high temperature/humidity for long periods.

(4) CAUTION FOR OPERATION

The viewing angle can be adjusted by varying the LCD driving voltage VLCD.

Driving voltage should be kept within specified range, excess voltage shortens display life.

Response time increases with decrease in temperature.

Display may turn black or dark Blue at temperature above its operational range; this is however not destructive and the display will return to normal once the temperature falls back to range.

Mechanical disturbance during operation (such as pressing on the viewing area) may cause the segments to appear “fractured”. They will recover once the display is turned off.

Condensation at terminals will cause malfunction and possible electrochemical reaction. Relative humidity of the environment should therefore be kept below 60%.

(5) SAFETY

Liquid crystal may leak out of a damaged LCD, it is recommended to wash off the liquid crystal by using solvents such as acetone or ethanol and should be burned up later.

If any liquid leaks out of a damaged glass cell comes in contact with your hands, wash it off with soap and water immediately.

WARRANTY

CLOVER will replace or repair any of her LCD module in accordance with her LCD specification for a period of one year from date of shipment. The warranty liability of Clover is limited to repair and/or replacement. Clover will not be responsible for any subsequent or consequential event.